



永源微电子科技有限公司

AP20G02BDF

20A 20V N+P 低功耗高频场效应管晶体管

简介:

AP20G02BDF 是一颗针对无线充 N+P 全桥高频电路高性价比产品，使用的是第三代沟槽技术，优化 N&P Ciss 电容数据和 RDS，在获取性价比同时，兼容了性能的提升。

适配主控型号:

IP6822 (英集芯)

20V N+P-Channel Enhancement Mode MOSFET

Description

The AP20G02BDF uses advanced **Trench III** technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 20V$ $I_D = 20A$

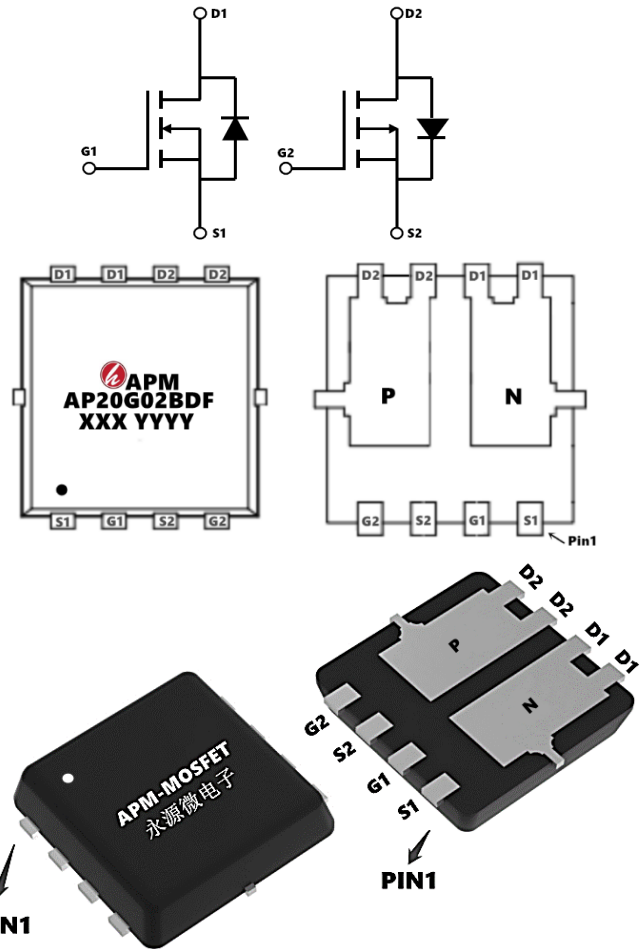
$R_{DS(ON)} < 18m\Omega$ @ $V_{GS}=10V$ (Type: 12m Ω)

$V_{DS} = -20V$ $I_D = -18.8A$

$R_{DS(ON)} < 30m\Omega$ @ $V_{GS}=-10V$ (Type: 25m Ω)

Application

High Frequency Circuit
low-power consumption



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP20G02BDF	PDFN3*3-8L	AP20G02BDF XXX YYYY	3000

Absolute Maximum Ratings ($T_c=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	N-Ch	P-Ch	Units
V_{DS}	Drain-Source Voltage	20	-20	V
V_{GS}	Gate-Source Voltage	± 12	± 12	V
$I_{D@T_A=25^\circ\text{C}}$	Continuous Drain Current, $V_{GS} @ 10V^1$	20	-18.8	A
$I_{D@T_A=70^\circ\text{C}}$	Continuous Drain Current, $V_{GS} @ 10V^1$	16.2	-15.5	A
IDM	Pulsed Drain Current ²	60	-54	A
EAS	Single Pulse Avalanche Energy ³	85	78	mJ
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation ⁴	3.5	3.5	W
TSTG	Storage Temperature Range	-55 to 150		$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150		$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	105		$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	50		$^\circ\text{C/W}$

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N-Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
BVDSS	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	20	23	-	V
IGSS	Gate Leakage Current	V _{GS} = ±12V, V _{DS} = 0V	-	-	±100	nA
IDSS	Drain Cut-off Current	V _{DS} = 20V, V _{GS} = 0V	-	-	1	μA
VGS(th)	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 250μA	0.4	0.7	1.2	V
RDS(on)	Drain-Source On-State Resistance ³	V _{GS} = 4.5V, I _D = 7.6A	-	11	23	mΩ
		V _{GS} = 2.5V, I _D = 3.5A	-	15	35	
Ciss	Input Capacitance	V _{GS} = 0V, V _{DS} = 10V, f = 1MHz	-	700	-	pF
Coss	Output Capacitance		-	120	-	
Crss	Reverse Transfer Capacitance		-	105	-	
Q _g	Total Gate Charge	V _{GS} = 4.5V, V _{DS} = 10V, I _D = 5A	-	9.6	-	nC
Q _{gs}	Gate-Source Charge		-	1.4	-	
Q _{gd}	Gate-Drain Charge		-	2.7	-	
td(on)	Turn-On Time	V _{GS} = 4.5V, V _{DD} = 10V, I _D = 5A, R _G = 3Ω	-	5.5	-	ns
t _r	Rise Time		-	1.3	-	
td(off)	Turn-Off Time		-	10.4	-	
t _f	Fall Time		-	4.8	-	
VSD	Body Diode Voltage ³	I _S = 4A, V _{GS} = 0V	-	-	1.2	V
IS	Continuous Source Current		-	-	5	A

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3、The power dissipation is limited by 150°C junction temperature
- 4、The EAS data shows Max. rating . The test condition is V_{DD}=18V,R_G=25Ω V_{GS}=4.5V,L=0.1mH,I_{AS}=11A
- 5、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

20V N+P-Channel Enhancement Mode MOSFET

P-Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = -250μA	-20	-23	-	V
IGSS	Gate-Body Leakage	V _{DS} = 0V, V _{GS} = ±12V	-	-	±100	nA
IDSS	Zero Gate Voltage Drain Current	V _{DS} = -20V, V _{GS} = 0V	-	-	-1	μA
VGS(th)	Gate-Threshold Voltage	V _{DS} = V _{GS} , I _D = -250μA	-0.4	-0.7	-1.2	V
RDS(on)	Drain-Source on-Resistance ³	V _{GS} = -4.5V, I _D = -4.1A	-	23	35	mΩ
		V _{GS} = -2.5V, I _D = -3.0A	-	41	57	
Ciss	Input Capacitance	V _{GS} = 0V, V _{DS} = -10V, f= 1MHz	-	751	-	pF
Coss	Output Capacitance		-	97	-	
Crss	Reverse Transfer Capacitance		-	80	-	
Q _g	Total Gate Charge	V _{GS} = -4.5V, V _{DS} = -10V, I _D = -4A	-	9.3	-	nC
Q _{gs}	Gate-Source Charge		-	1	-	
Q _{gd}	Gate-Drain Charge		-	2.2	-	
td(on)	Turn-on Delay Time	V _{GS} = -4.5V, V _{DS} = -10V, R _G = 3Ω, I _D = -4A	-	13	-	ns
t _r	Rise time		-	9	-	
td(off)	Turn-off Delay Time		-	19	-	
t _f	Fall Time		-	29	-	
VSD	Body Diode Voltage ³	I _S = -1A, V _{GS} = 0V	-	-	-1	V
IS	Continuous Source Current		-	-	-4.1	A

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3、The power dissipation is limited by 150°C junction temperature
- 4、The EAS data shows Max. rating . The test condition is V_{DD}=18V,R_G=25Ω V_{GS}=4.5V,L=0.1mH,I_{AS}=18A
- 5、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

N-Typical Characteristics

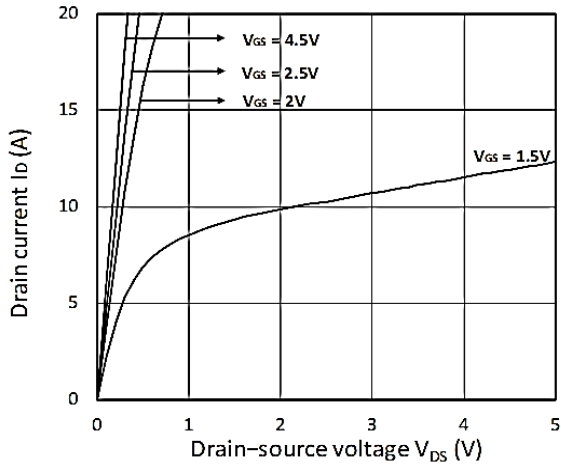


Figure 1. Output Characteristics

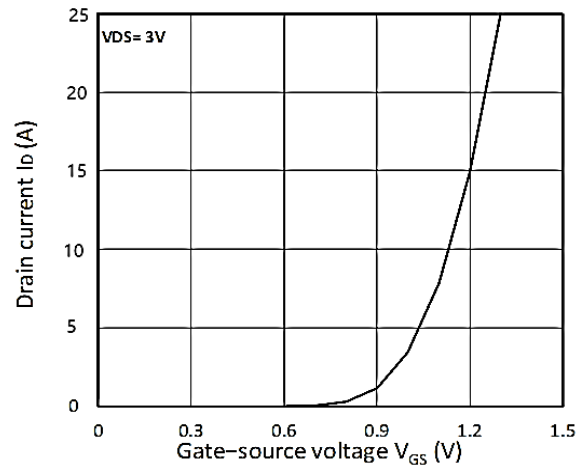


Figure 2. Transfer Characteristics

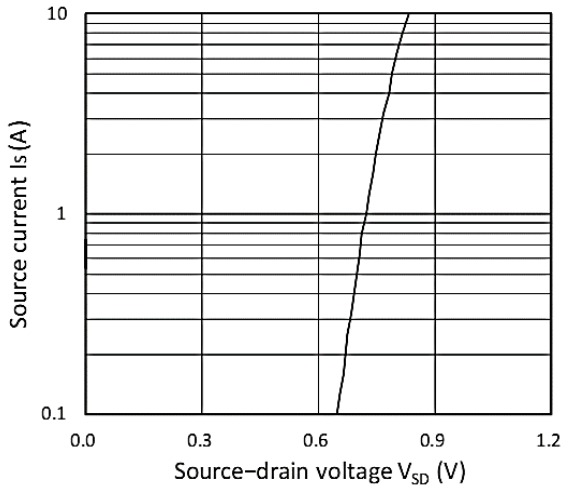


Figure 3. Forward Characteristics of Reverse

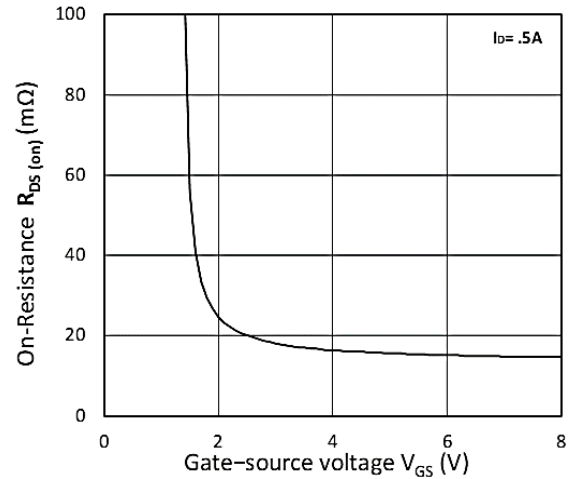


Figure 4. R_DS(ON) vs. V_GS

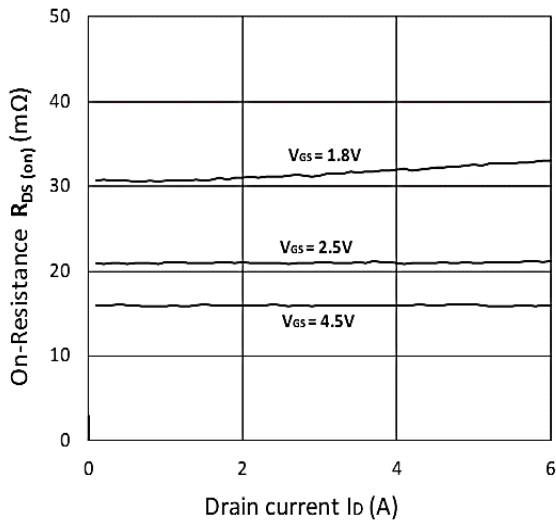


Figure 5. R_DS(ON) vs. I_D

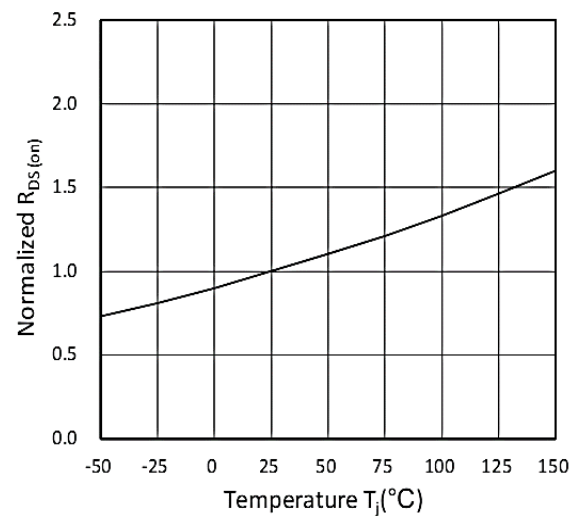


Figure 6. Normalized R_DS(on) vs. Temperature

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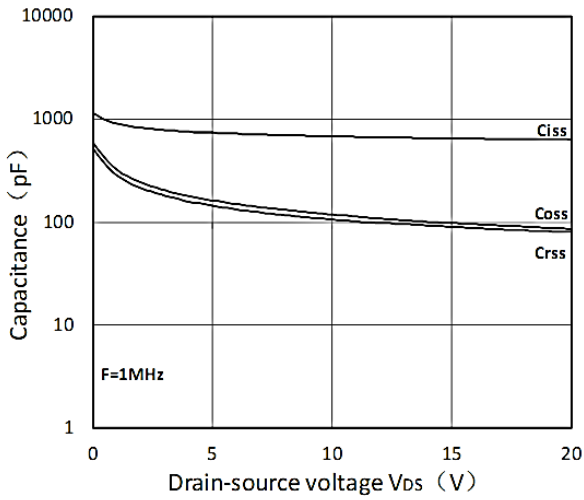


Figure 7. Capacitance Characteristics

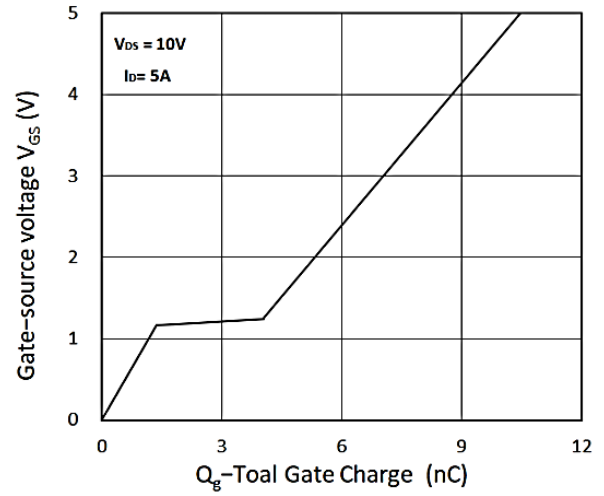


Figure 8. Gate Charge Characteristics

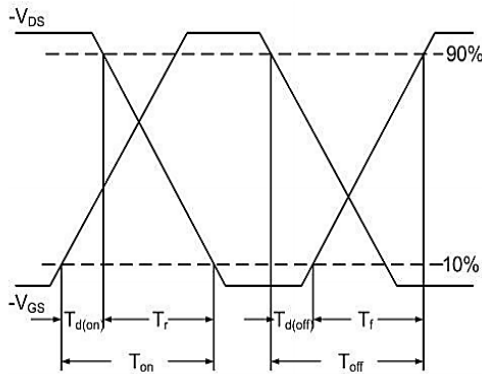


Figure.9 Switching Time Waveform

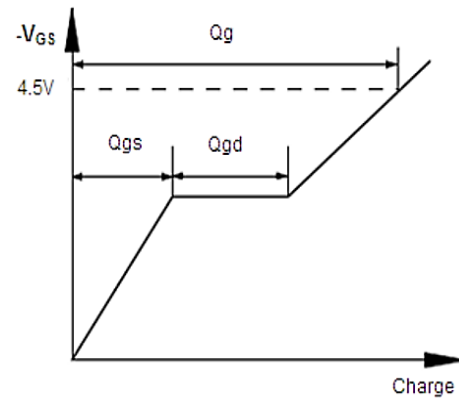


Figure.10 Gate Charge Waveform

P-Typical Characteristics

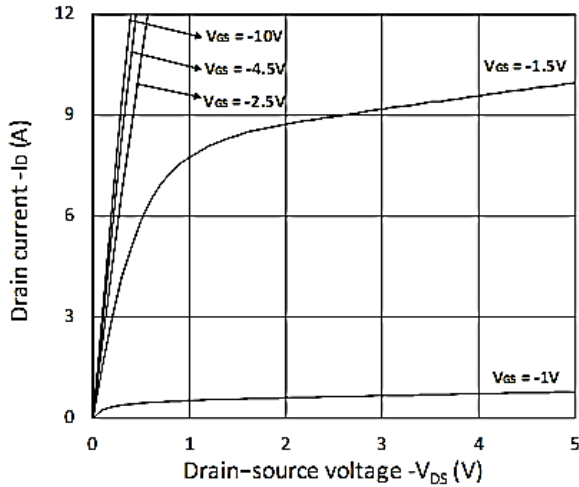


Figure 1. Output Characteristics

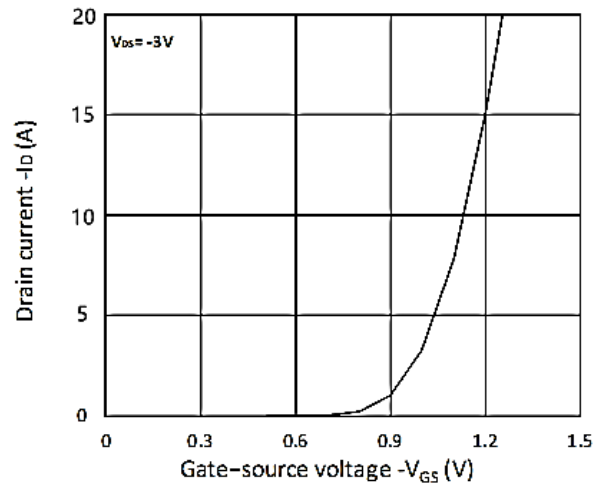


Figure 2. Transfer Characteristics

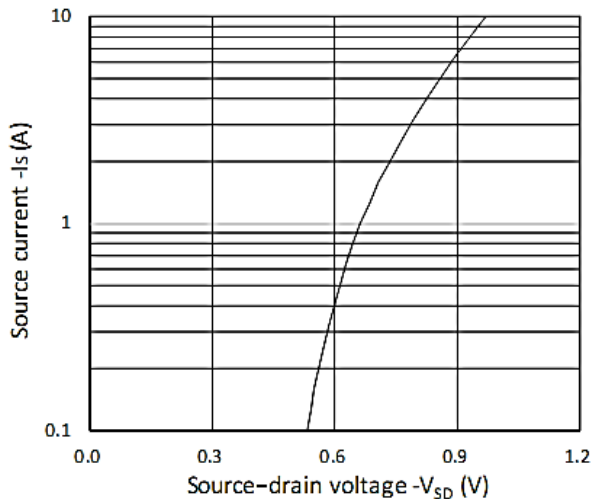


Figure 3. Forward Characteristics of Reverse

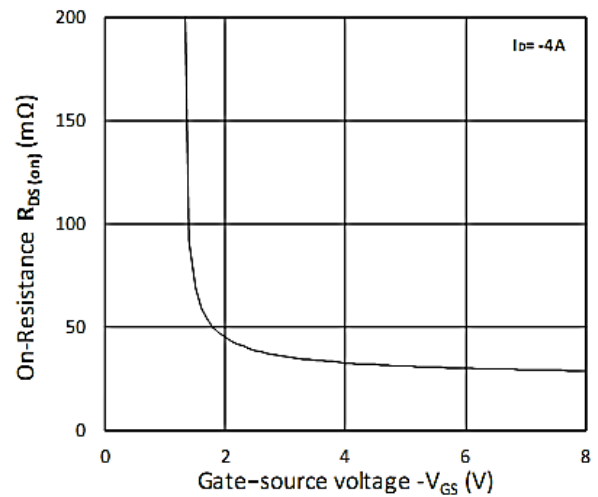


Figure 4. R_DS(ON) vs. V_GS

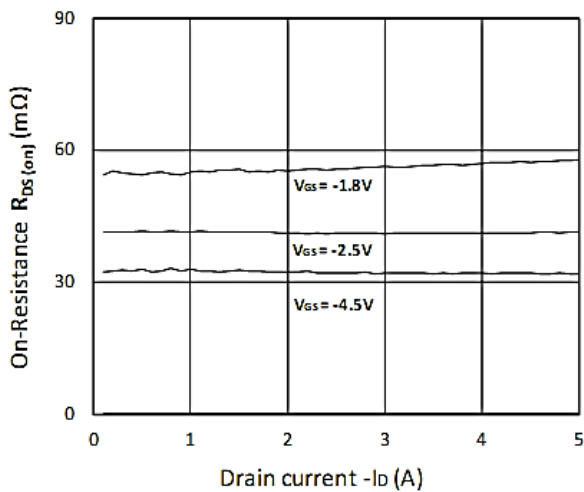


Figure 5. R_DS(ON) vs. I_D

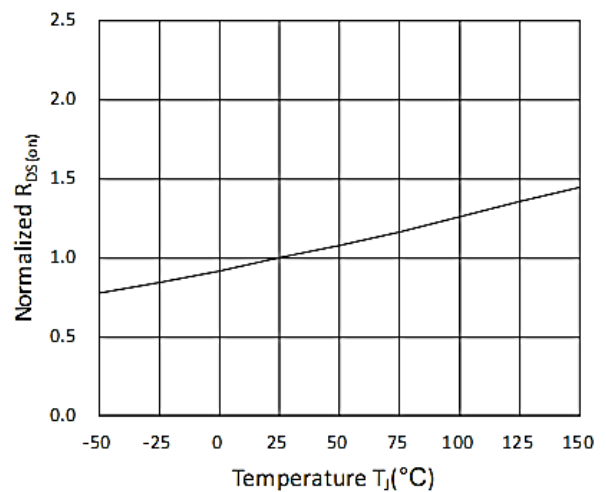


Figure 6. Normalized R_DS(on) vs. Temperature

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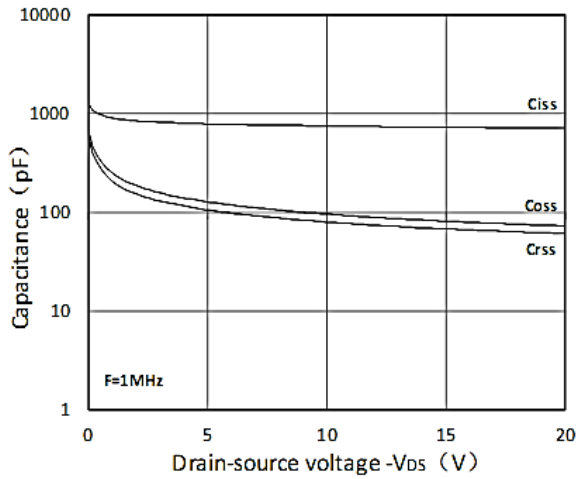


Figure 7. Capacitance Characteristics

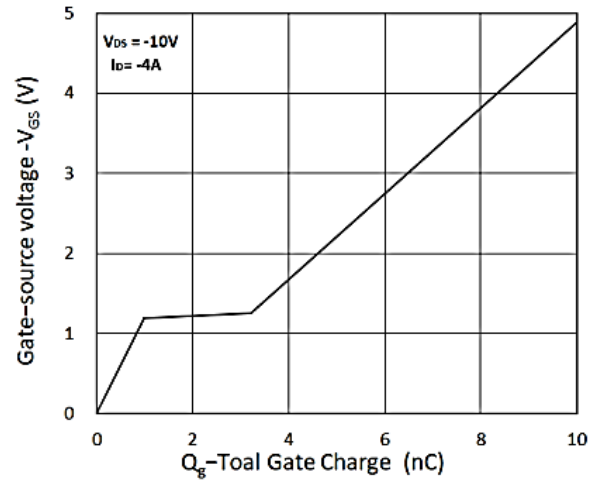


Figure 8. Gate Charge Characteristics

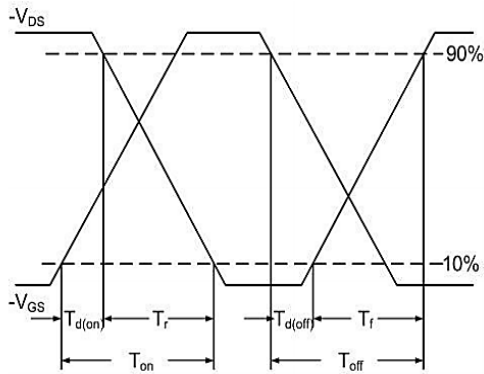


Figure.9 Switching Time Waveform

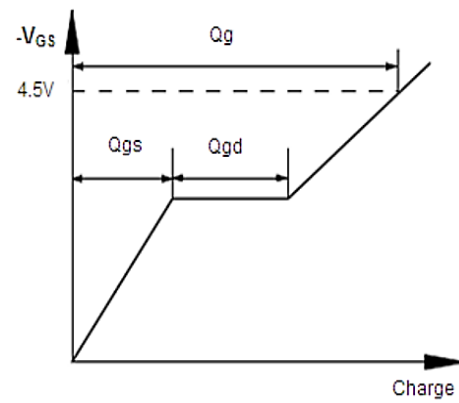
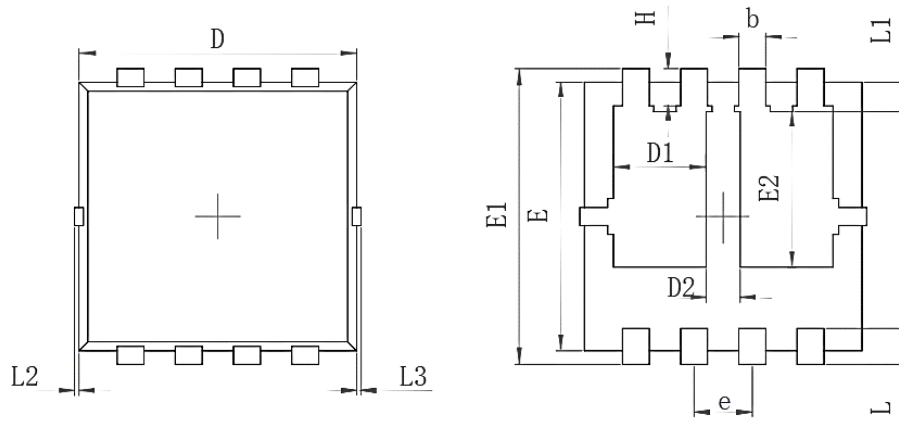
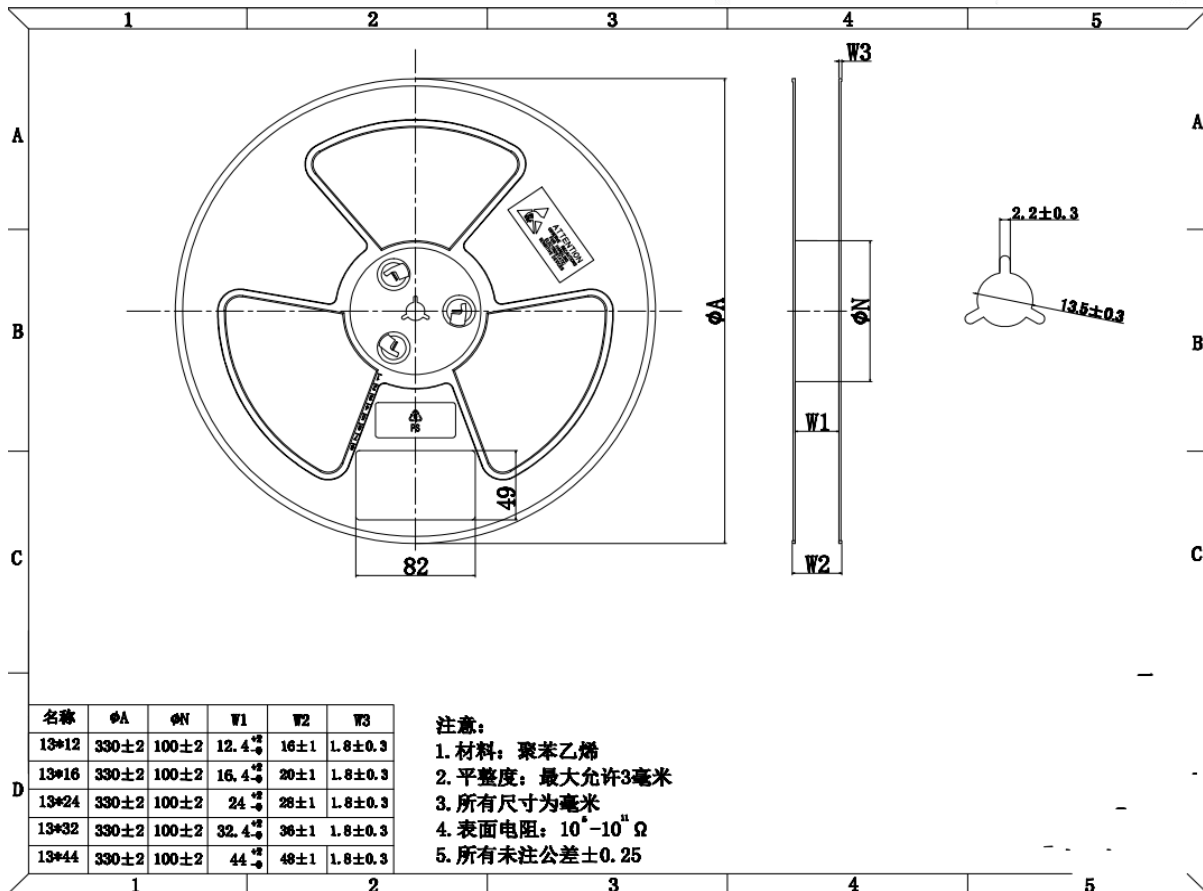
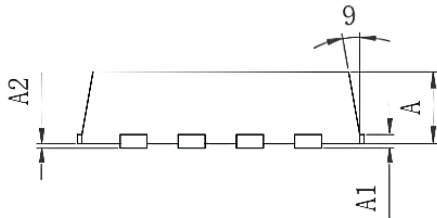


Figure.10 Gate Charge Waveform

Package Mechanical Data-PDFN3*3-8L Double



SYMBOL	MILLIMETER	
	MIN	MAX
A	0.700	0.900
A1	0.152 REF.	
A2	0°0.05	
D	3.000	3.200
D1	0.935	1.135
D2	0.280	0.480
E	2.900	3.100
E1	3.150	3.450
E2	1.535	1.935
b	0.200	0.400
e	0.550	0.750
L	0.300	0.500
L1	0.180	0.480
L2	0°0.100	
L3	0°0.100	
H	0.315	0.515
9	8°	12°



20V N+P-Channel Enhancement Mode MOSFET**Attention**

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20V N+P-Channel Enhancement Mode MOSFET

Edition	Date	Change
REV1.0	2023/3/21	Initial release
REV1.1	2023/8/18	Optimize Ciss and RDS

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