

-30V P-Channel Enhancement Mode MOSFET

Description

The AP3401BI uses advanced Trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

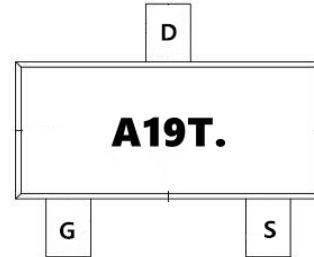
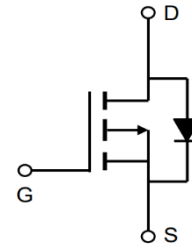
$V_{DS} = -30V$ $I_D = -4.2A$

$R_{DS(ON)} < 55m\Omega$ @ $V_{GS}=10V$ (Type: 45m Ω)

$R_{DS(ON)} < 68m\Omega$ @ $V_{GS}=4.5V$ (Type: 53m Ω)

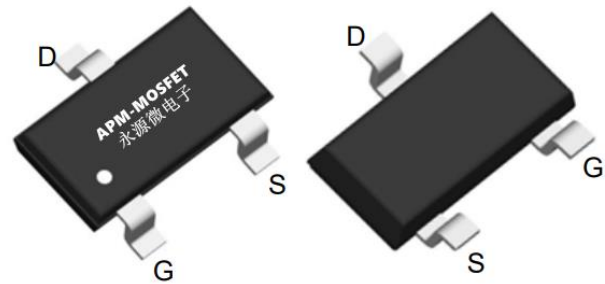
Application

Battery protection
Load switch
Uninterruptible power supply



Top View

Bottom View



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP3401BI	SOT23L	A19T.	3000

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Max.	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	± 12	V
$I_D @ T_C=25^{\circ}C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-4.2	A
$I_D @ T_C=100^{\circ}C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-2.7	A
IDM	Pulsed Drain Current ^{note1}	-16.8	A
P_D	Power Dissipation $T_A = 25^{\circ}C$	1.5	W
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	125	$^{\circ}C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	104	$^{\circ}C/W$
TJ, TSTG	Operating and Storage Temperature Range	-55 to +150	$^{\circ}C$

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Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D = -250μA	-30	-	-	V
IDSS	Zero Gate Voltage Drain Current	V _{DS} = -30V, V _{GS} =0V,	-	-	-1	μA
IGSS	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} = ±12V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250μA	-0.5	-0.9	-1.5	V
RDS(on)	Static Drain-Source on-Resistance note2	V _{GS} = -10V, I _D = -4A	-	45	55	mΩ
		V _{GS} = -4.5V, I _D = -3A	-	53	68	
		V _{GS} = -2.5V, I _D = -1A	-	72	96	V
Ciss	Input Capacitance	V _{DS} = -15V, V _{GS} =0V, f=1.0MHz	-	500	-	pF
Coss	Output Capacitance		-	80	-	pF
Crss	Reverse Transfer Capacitance		-	2	-	pF
Q _g	Total Gate Charge	V _{DS} = -15V, I _D = -4.2A, V _{GS} = -10V	-	8.5	-	nC
Q _{gs}	Gate-Source Charge		-	1.8	-	nC
Q _{gd}	Gate-Drain("Miller") Charge		-	2.7	-	nC
td(on)	Turn-on Delay Time	V _{DD} = -15V, I _D = -1A, V _{GS} = -10V, R _{GEN} =2.5Ω	-	7	-	ns
tr	Turn-on Rise Time		-	3	-	ns
td(off)	Turn-off Delay Time		-	20	-	ns
tf	Turn-off Fall Time		-	12	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	-4.2	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-16.8	A
VSD	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S = -4.2A	-	-0.8	-1.2	V

Note :

- 1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 20Z copper.
- 2、The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
- 3、The power dissipation is limited by 150°C junction temperature
- 4、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

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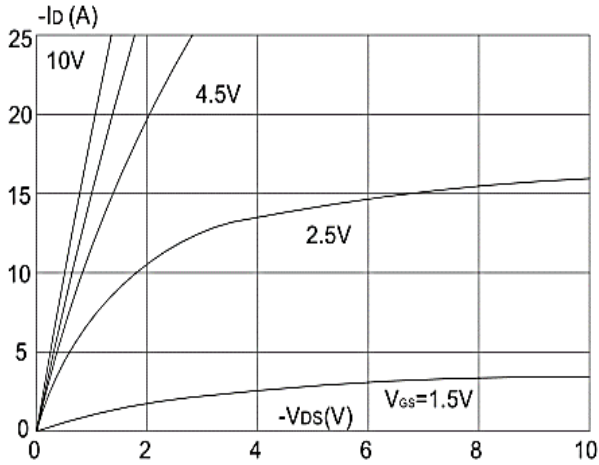


Figure1: Output Characteristics

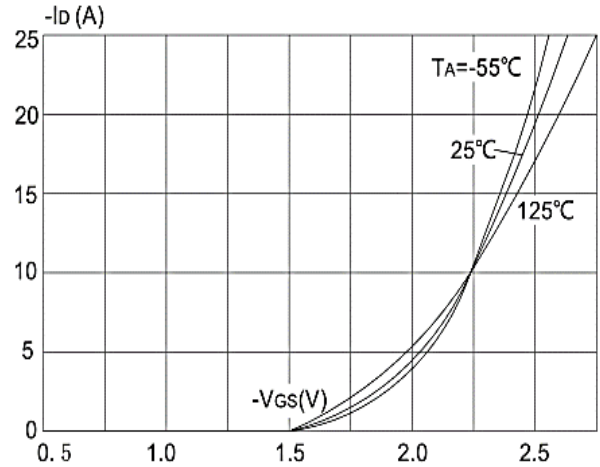


Figure 2: Typical Transfer Characteristics

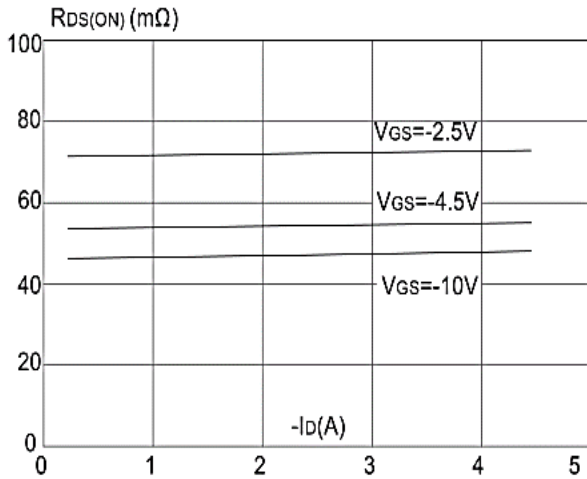


Figure 3: On-resistance vs. Drain Current

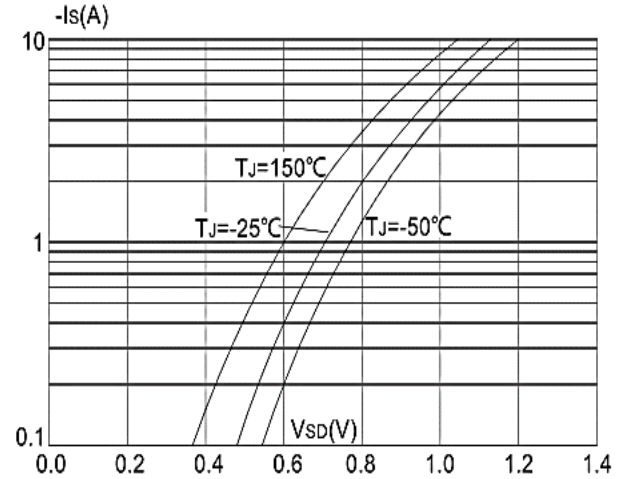


Figure 4: Body Diode Characteristics

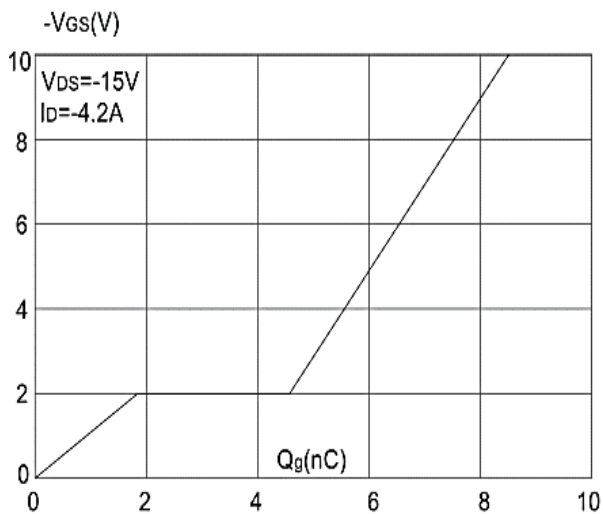


Figure 5: Gate Charge Characteristics

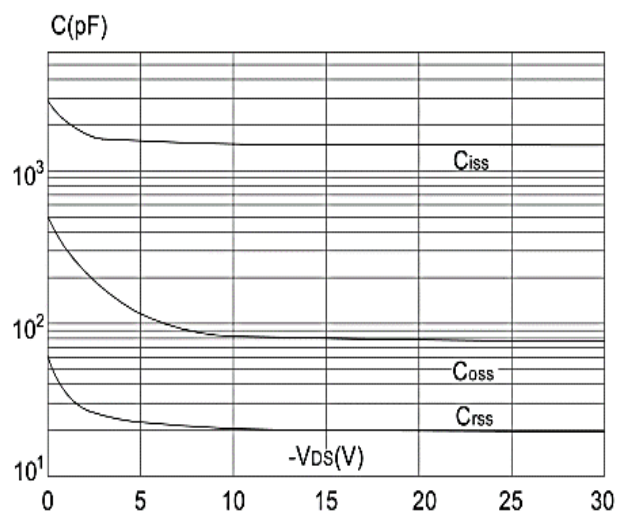


Figure 6: Capacitance Characteristics

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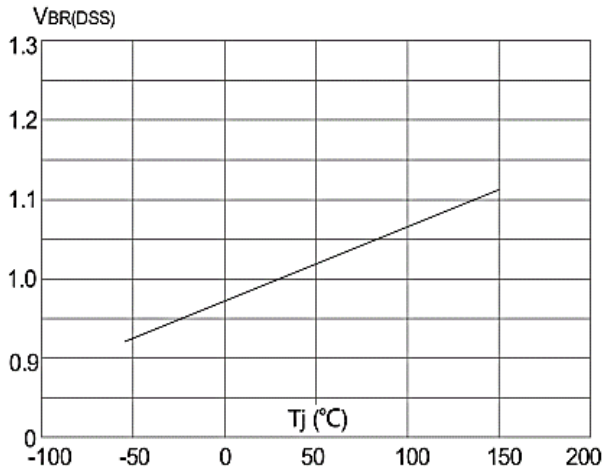


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

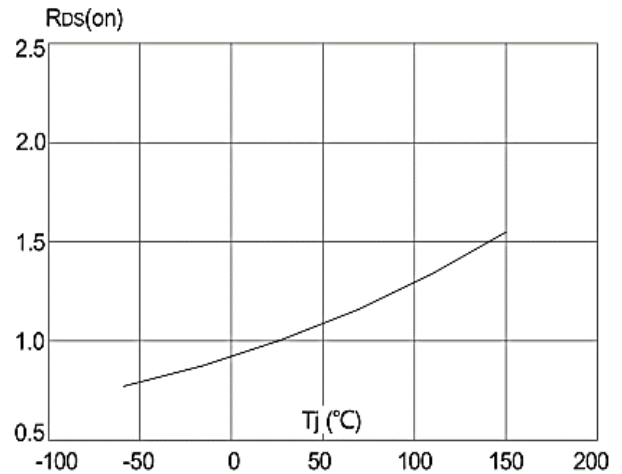


Figure 8: Normalized on Resistance vs. Junction Temperature

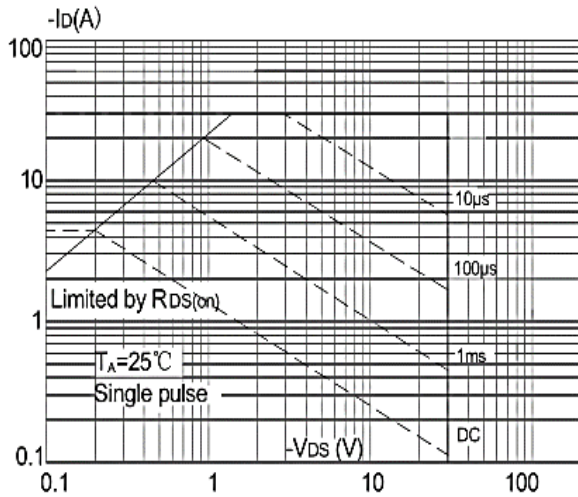


Figure 9: Maximum Safe Operating Area

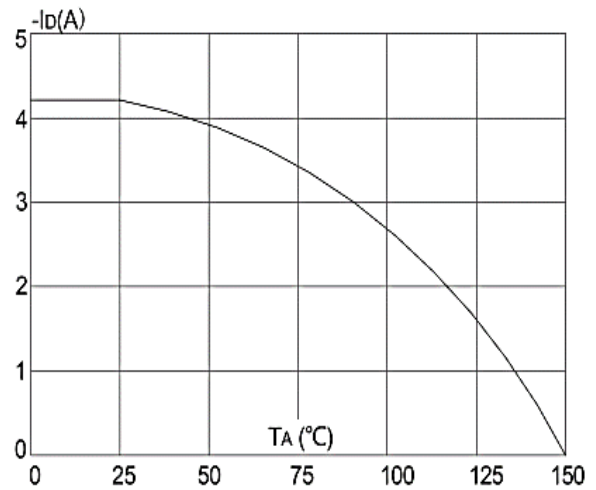


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

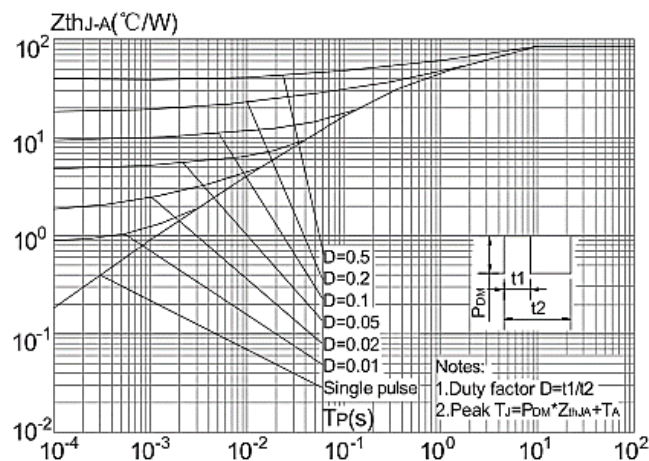
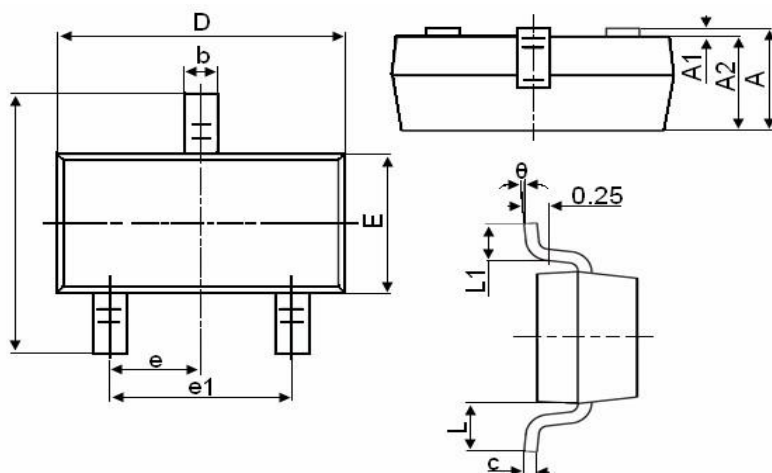


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

Package Mechanical Data-SOT23-XC-Single



Symbol	Dimensions in Millimeters	
	MIN.	MAX.
A	0.900	1.150
A1	0.000	0.100
A2	0.900	1.050
b	0.300	0.500
c	0.080	0.150
D	2.800	3.000
E	1.200	1.400
E1	2.250	2.550
e	0.950TYP	
e1	1.800	2.000
L	0.550REF	
L1	0.300	0.500
θ	0°	8°

-30V P-Channel Enhancement Mode MOSFET**Attention**

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AP3401BI**-30V P-Channel Enhancement Mode MOSFET**

Edition	Date	Change
Rve1.0	2018/11/31	Initial release
Rve1.1	2021/12/10	Reduce internal RDS

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