

30V N+P-Channel Enhancement Mode MOSFET

Description

The AP8G03S uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 30V$ $I_D = 9.8A$

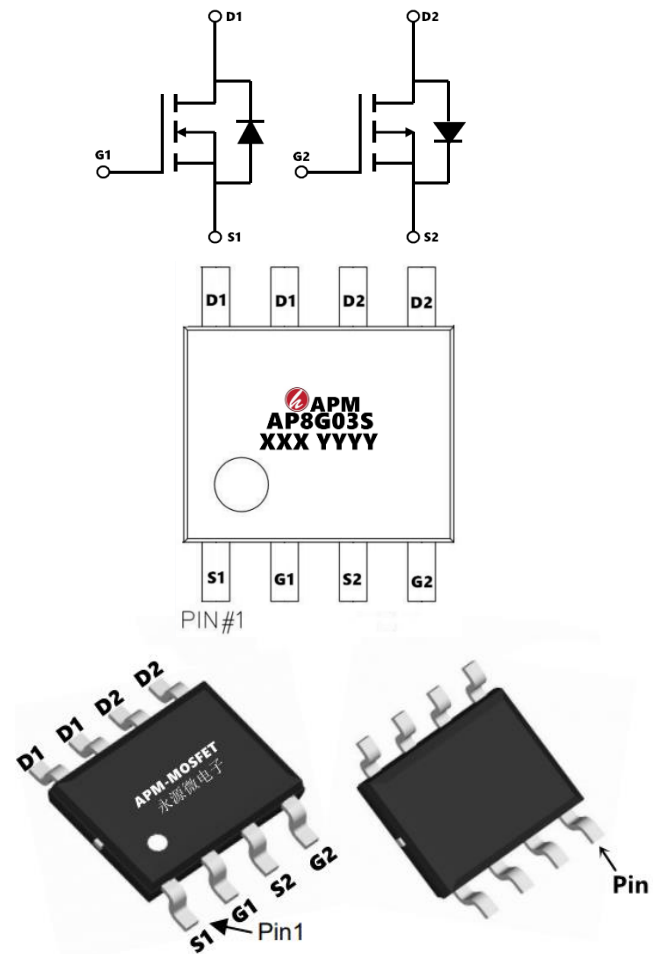
$R_{DS(ON)} < 25m\Omega$ @ $V_{GS}=10V$ (Type: 16m Ω)

$V_{DS} = -30V$ $I_D = -9.8A$

$R_{DS(ON)} < 25m\Omega$ @ $V_{GS}=-10V$ (Type: 16m Ω)

Application

BLDC



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP8G03S	SOP-8L	AP8G03S XXX YYYY	3000

Absolute Maximum Ratings ($T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	N-Ch	P-Ch	Units
V_{DS}	Drain-Source Voltage	30	-30	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D @ T_A=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	9.8	-9.8	A
$I_D @ T_A=70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	6.3	-6.3	A
I_{DM}	Pulsed Drain Current ²	29	-29	A
EAS	Single Pulse Avalanche Energy ³	80	80	mJ
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation ⁴	46	46	W
T_{STG}	Storage Temperature Range	-55 to 150		$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150		$^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	85		$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	40		$^\circ\text{C/W}$

30V N+P-Channel Enhancement Mode MOSFET
N-Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=250\mu A$	30	35	---	V
$\Delta BV_{DSS}/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=1mA$	---	0.023	---	V/ $^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V$, $I_D=5A$	---	16	25	m Ω
		$V_{GS}=4.5V$, $I_D=3A$	---	24	35	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu A$	1.2	1.6	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-4.2	---	mV/ $^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=24V$, $V_{GS}=0V$, $T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=24V$, $V_{GS}=0V$, $T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V$, $I_D=6A$	---	5.8	---	S
R_g	Gate Resistance	$V_{DS}=0V$, $V_{GS}=0V$, $f=1MHz$	---	2.3	---	Ω
Q_g	Total Gate Charge (4.5V)	$V_{DS}=20V$, $V_{GS}=4.5V$, $I_D=6A$	---	5	---	nC
Q_{gs}	Gate-Source Charge		---	1.11	---	
Q_{gd}	Gate-Drain Charge		---	2.61	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=12V$, $V_{GS}=10V$, $R_G=3.3\Omega$ $I_D=6A$	---	7.7	---	ns
T_r	Rise Time		---	46	---	
$T_{d(off)}$	Turn-Off Delay Time		---	11	---	
T_f	Fall Time		---	3.6	---	
C_{iss}	Input Capacitance	$V_{DS}=15V$, $V_{GS}=0V$, $f=1MHz$	---	416	---	pF
C_{oss}	Output Capacitance		---	62	---	
C_{rss}	Reverse Transfer Capacitance		---	51	---	
I_S	Continuous Source Current ^{1,6}	$V_G=V_D=0V$, Force Current	---	---	6.2	A
I_{SM}	Pulsed Source Current ^{2,6}		---	---	24	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=1A$, $T_J=25^\circ\text{C}$	---	---	1.2	V

Note :

- 1、The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3、The power dissipation is limited by 175°C junction temperature
- 4、The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

30V N+P-Channel Enhancement Mode MOSFET

P-Channel Electrical Characteristics (T_J=25°C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D = -250μA	-30	-33	-	V
IDSS	Zero Gate Voltage Drain Current	V _{DS} = -30V, V _{GS} =0V,	-	-	-1	μA
IGSS	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} = ±20V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D = -250μA	-1.2	-1.5	-2.5	V
RDS(on)	Static Drain-Source on-Resistance note3	V _{GS} = -10V, I _D = -10A	-	16	25	mΩ
		V _{GS} = -4.5V, I _D = -5A	-	25	30	
C _{iss}	Input Capacitance	V _{DS} = -15V, V _{GS} =0V, f=1.0MHz	-	1250	-	pF
C _{oss}	Output Capacitance		-	327	-	pF
C _{rss}	Reverse Transfer Capacitance		-	278	-	pF
Q _g	Total Gate Charge	V _{DS} = -15V, I _D = -9.1A, V _{GS} = -10V	-	30	-	nC
Q _{gs}	Gate-Source Charge		-	5.3	-	nC
Q _{gd}	Gate-Drain("Miller") Charge		-	7.6	-	nC
td(on)	Turn-on Delay Time	V _{DD} = -15V, I _D = -6A, V _{GS} = -10V, R _{GEN} =2.5Ω	-	14	-	ns
t _r	Turn-on Rise Time		-	20	-	ns
td(off)	Turn-off Delay Time		-	95	-	ns
t _f	Turn-off Fall Time		-	65	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	-10	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-40	A
VSD	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S = -11A	-	-0.8	-1.2	V

Note :

- 1、The data tested by surface mounted on a 1 inch 2 FR-4 board with 20Z copper.
- 2、The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3、The power dissipation is limited by 150°C junction temperature
- 4、The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

30V N+P-Channel Enhancement Mode MOSFET

N-Channel Typical Characteristics

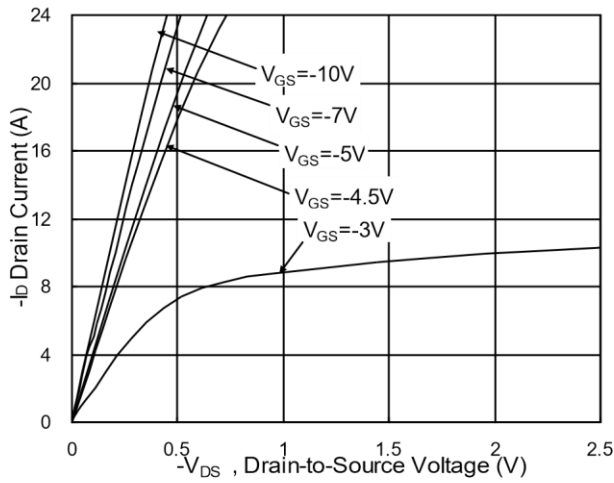


Fig.1 Typical Output Characteristics

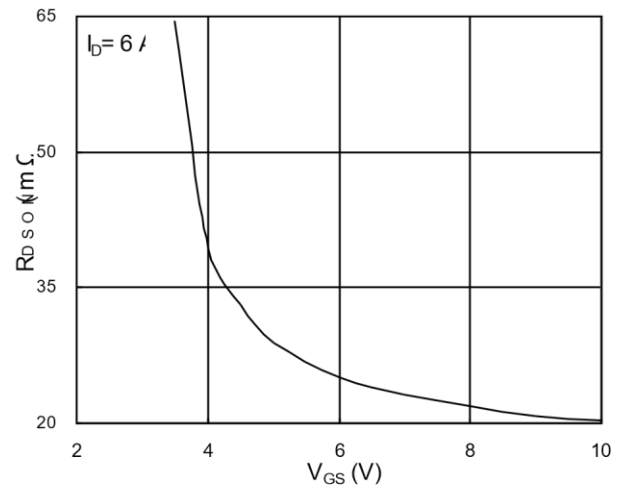


Fig.2 On-Resistance vs. Gate-Source

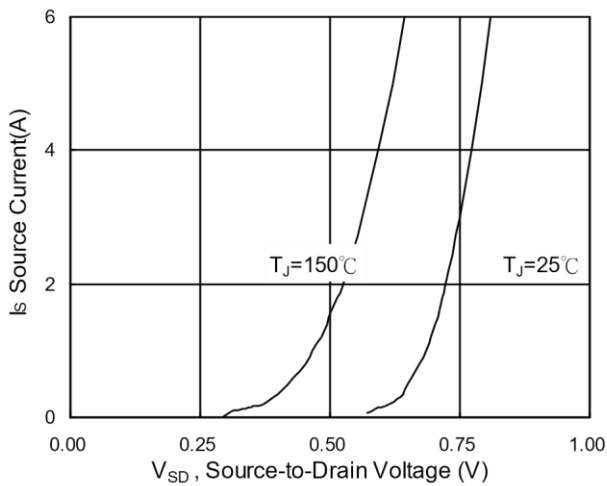


Fig.3 Forward Characteristics Of Reverse

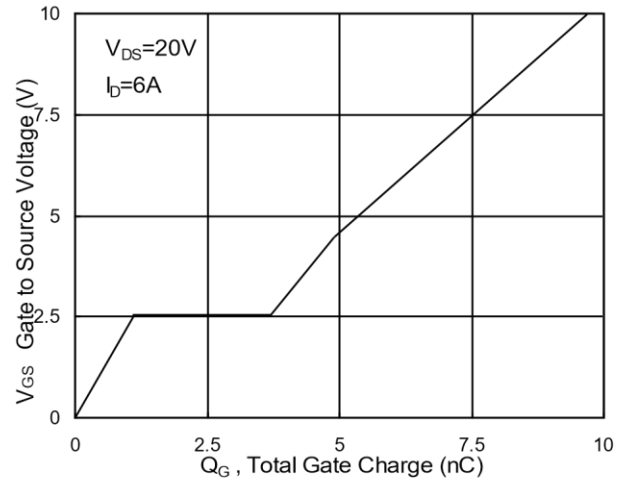


Fig.4 Gate-Charge Characteristics

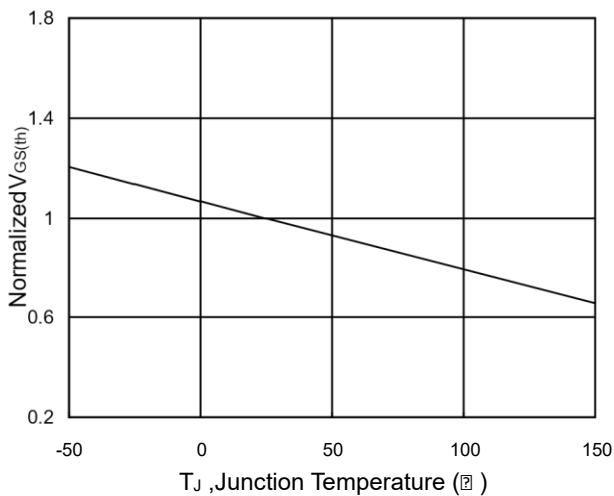


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

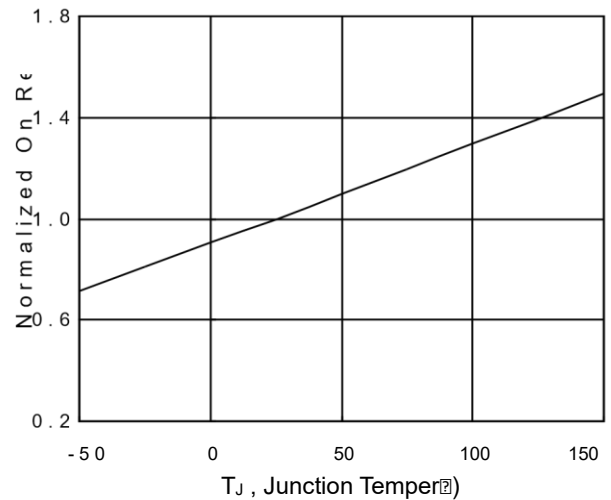


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

30V N+P-Channel Enhancement Mode MOSFET

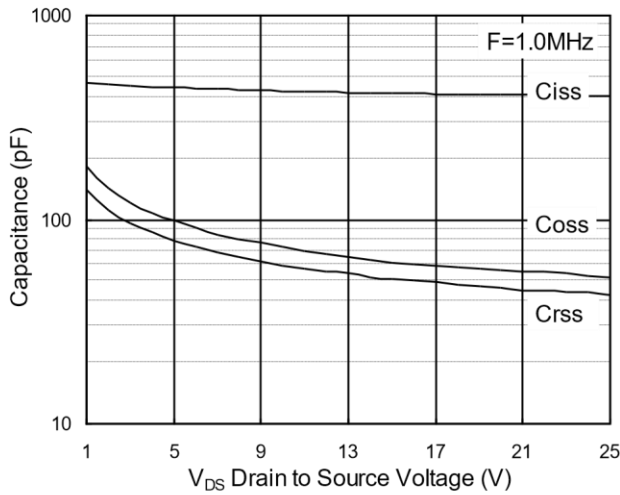


Fig.7 Capacitance

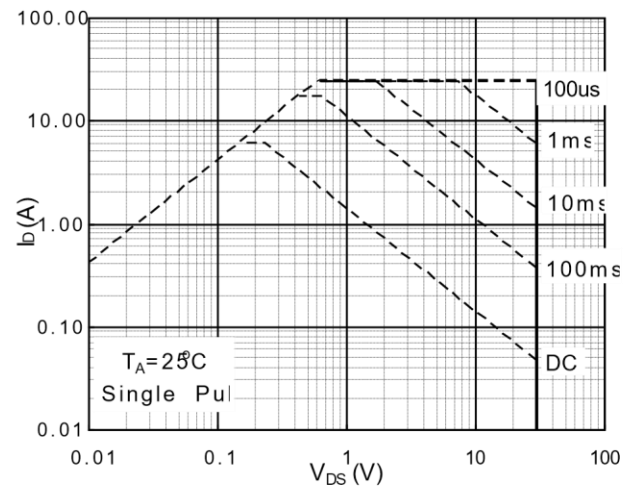


Fig.8 Safe Operating Area

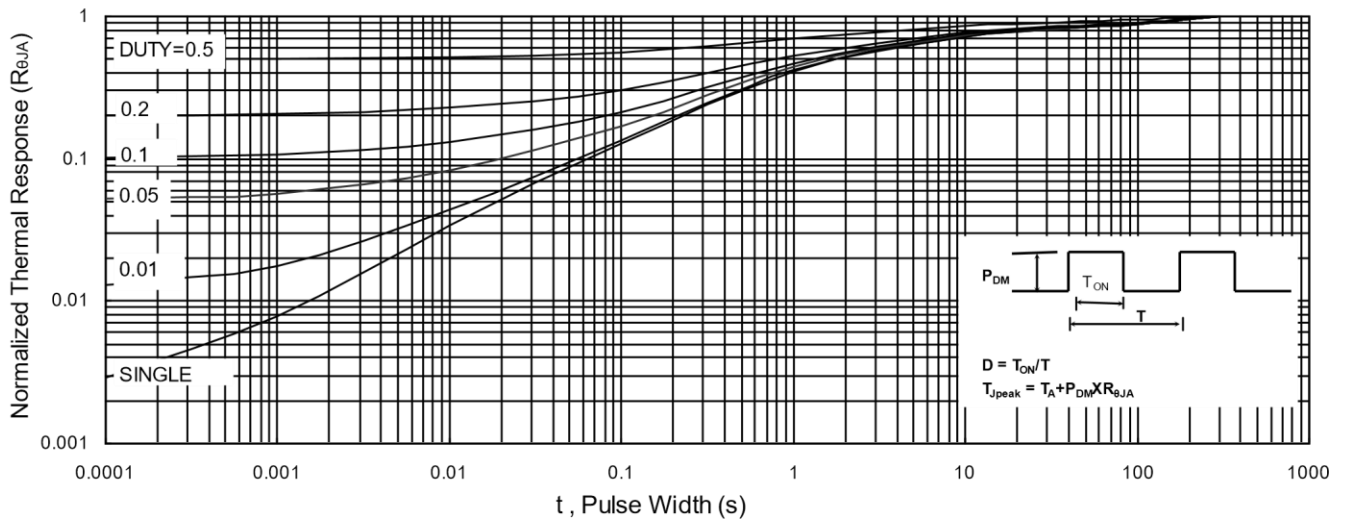


Fig.9 Normalized Maximum Transient Thermal Impedance

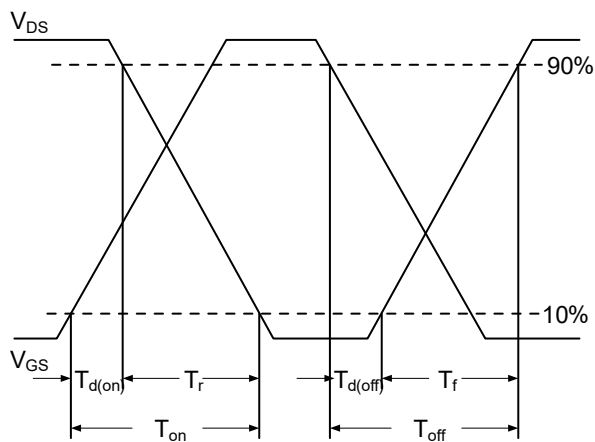


Fig.10 Switching Time Waveform

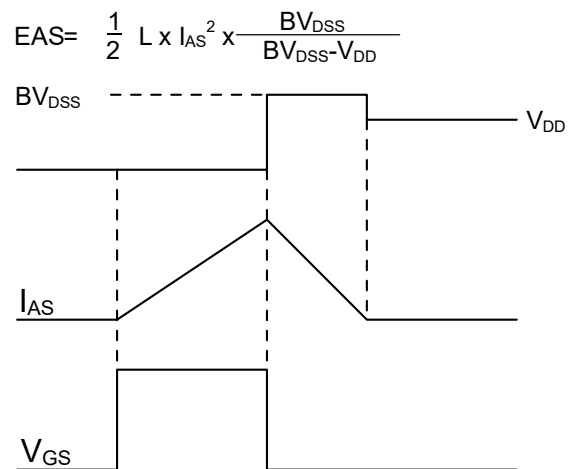


Fig.11 Unclamped Inductive Switching Waveform

30V N+P-Channel Enhancement Mode MOSFET

P-Channel Typical Characteristics

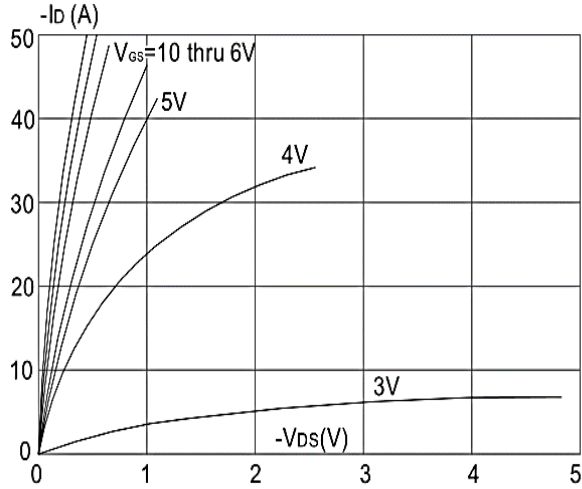


Figure1: Output Characteristics

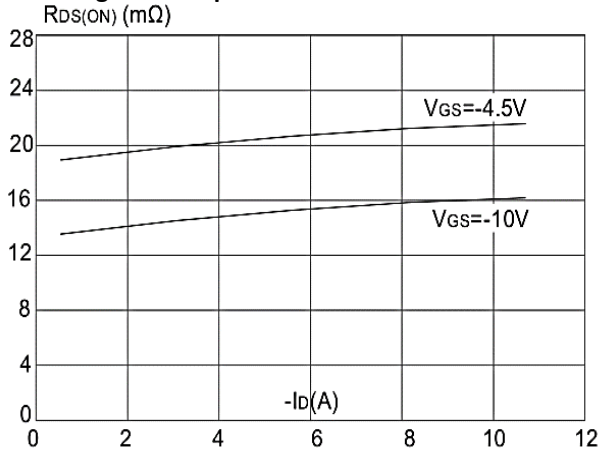


Figure 3: On-resistance vs. Drain Current

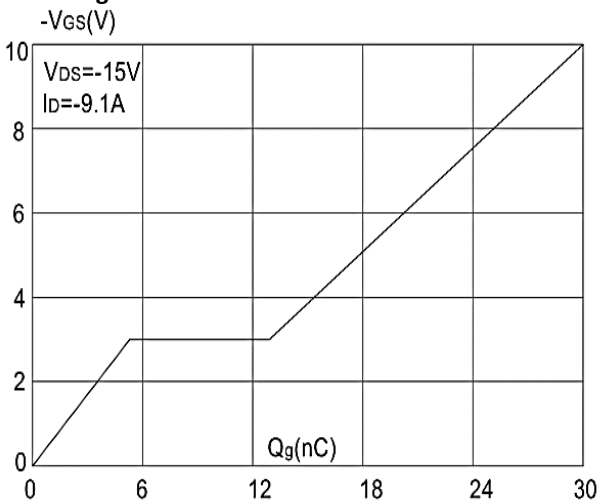


Figure 5: Gate Charge Characteristics

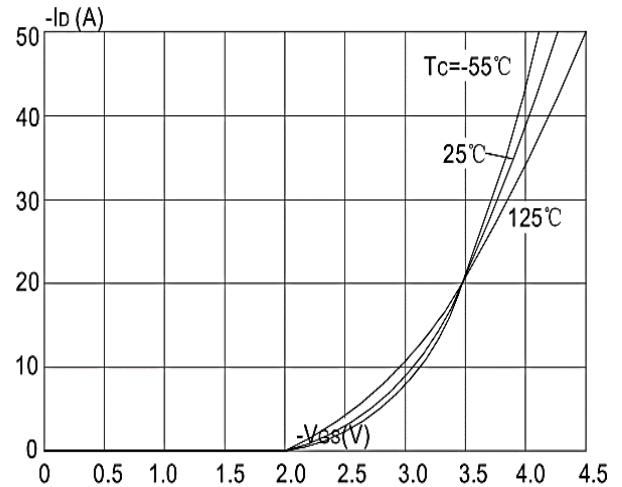


Figure 2: Typical Transfer Characteristics

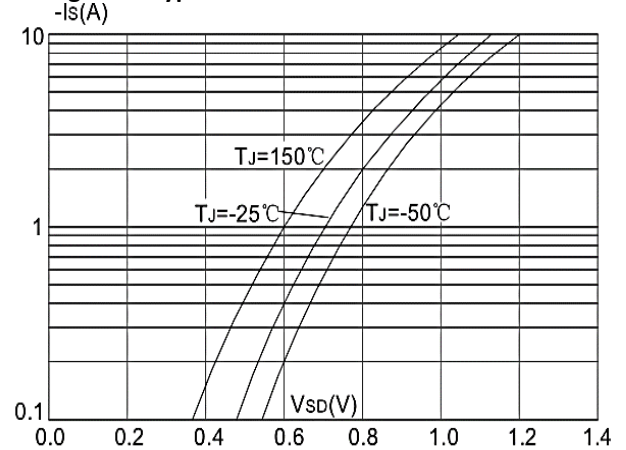


Figure 4: Body Diode Characteristics

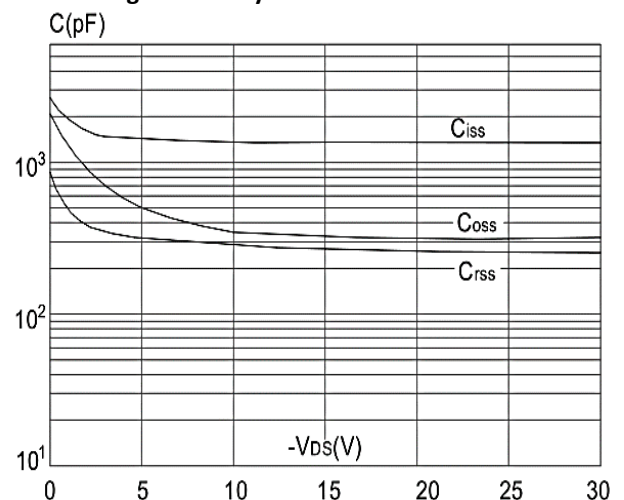


Figure 6: Capacitance Characteristics

30V N+P-Channel Enhancement Mode MOSFET

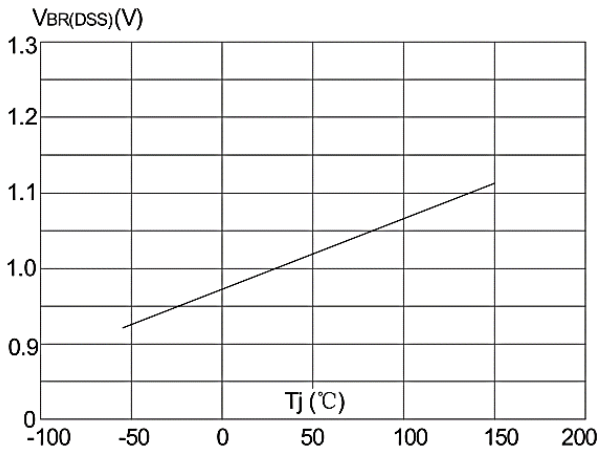


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

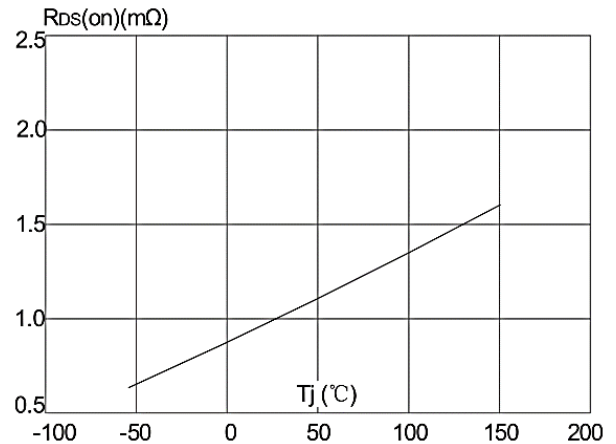


Figure 8: Normalized on Resistance vs. Junction Temperature

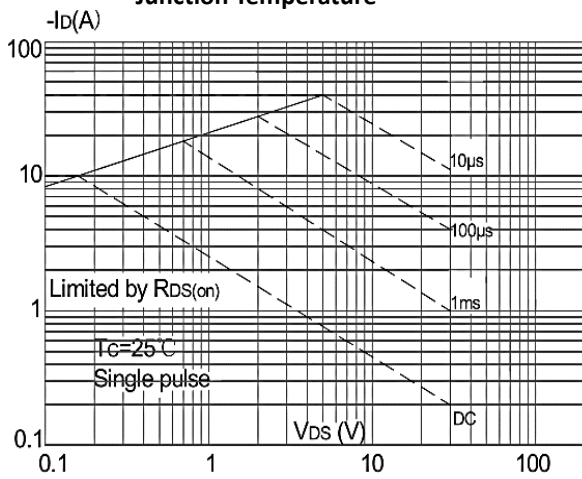


Figure 9: Maximum Safe Operating Area

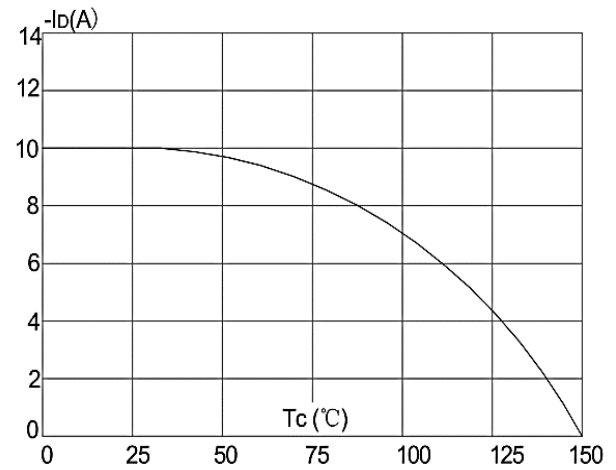


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

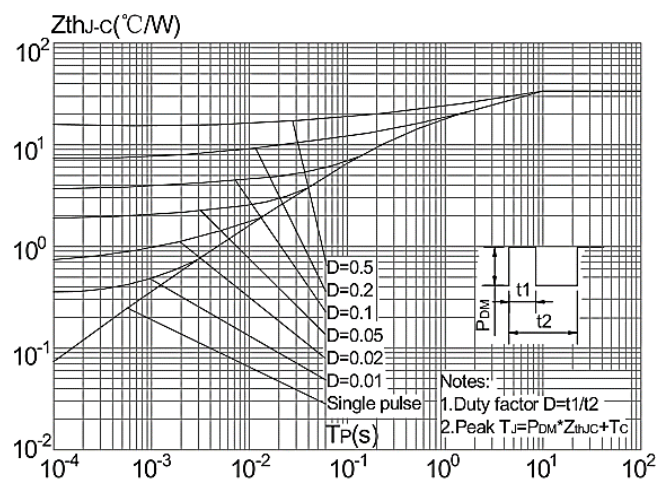
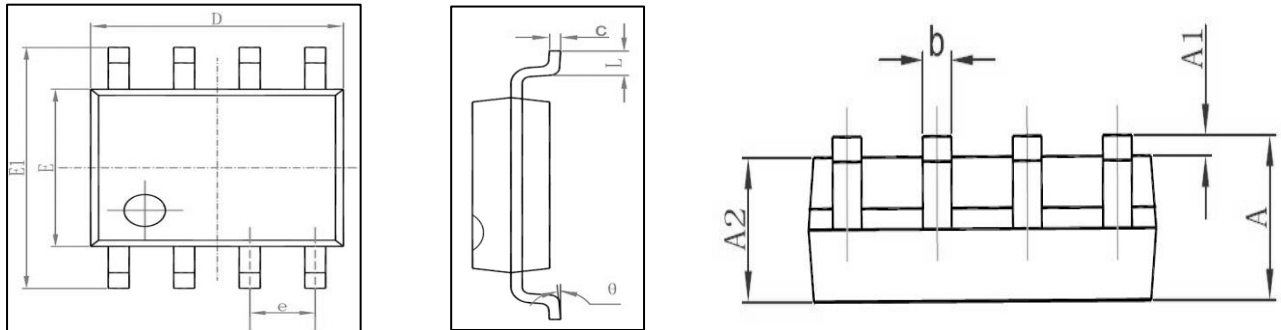


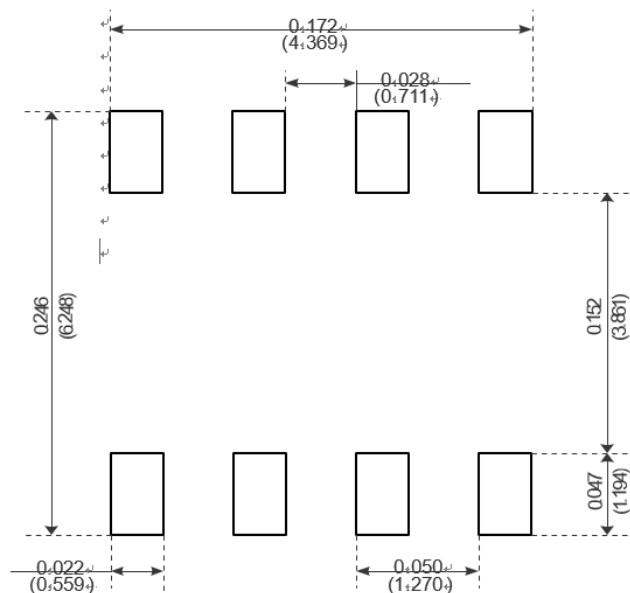
Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

30V N+P-Channel Enhancement Mode MOSFET

Package Mechanical Data-SOP-8L-DX-Double



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Recommended Minimum Pads

30V N+P-Channel Enhancement Mode MOSFET**Attention**

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Edition	Date	Change
RVE1.0	2021/1/31	Initial release

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