低电荷注入、16通道、带泄放电阻高压模拟开关

特性：

- ▶高性能的高压CMOS技术
- ▶输出集成泄放电阻
- ▶16通道高压模拟开关
- ▶ 3.3V输入逻辑电平兼容
- ▶20兆赫数据移位时钟频率
- ▶非常低的静态功耗（<25微安）
- ▶低寄生电容
- ▶直流至50兆赫小信号频率响应
- ▶ -5.0兆赫时的典型断开隔离-60dB
- ▶用于低功耗的CMOS逻辑电路
- ▶卓越的抗噪性
- ▶带锁存器的级联串行数据寄存器
- ▶灵活的工作电源电压

概述：

SY2160为低电荷注入，16通道，高压模拟开关集成电路。这芯片是为以下应用而设计的需要低压信号控制的高压开关，如医学超声图像、工业无损探伤和其他压电传感器驱动器。SY2160集成了泄放电阻，用来消除电容性负载（如压电传感器）两端积累噪声电压

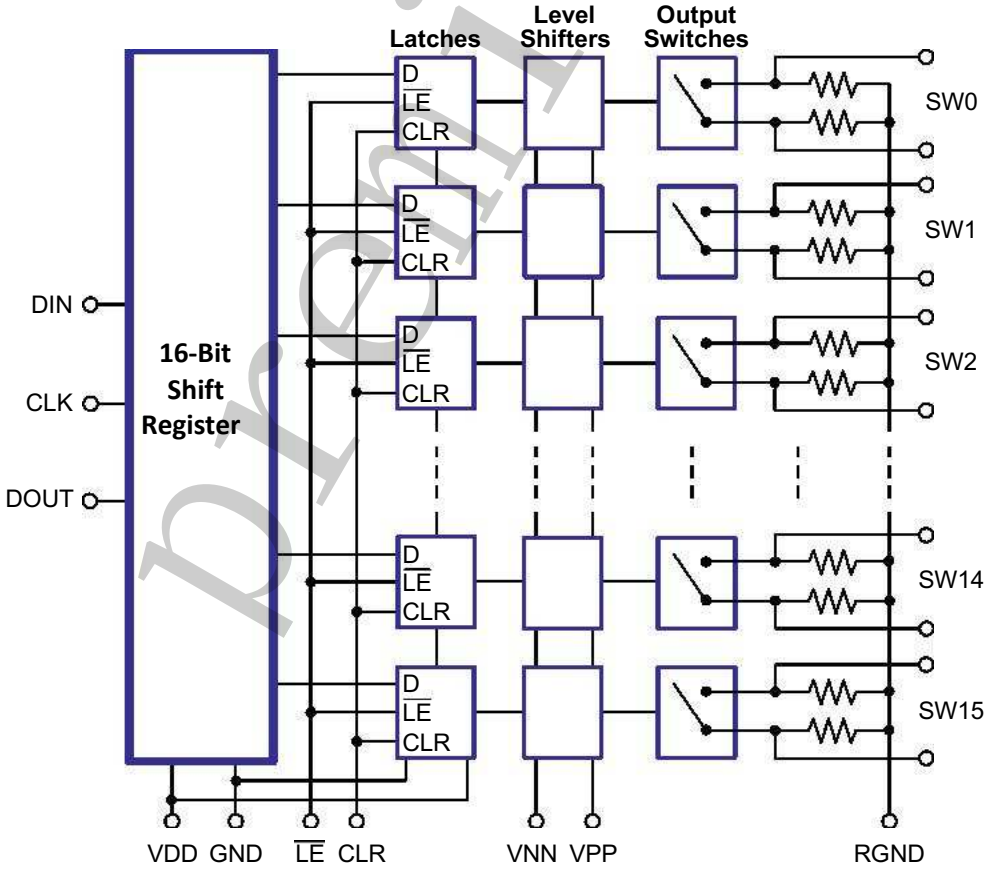
该器件将输入数据移位到16位移位寄存器中，然后可以保留在16位锁存器中。为了减少时钟馈通引入的噪声，在数据载入移位寄存器期间将LE拉至高电平。当移位寄存器 装载有效数据后，在LE作用一个低电平脉冲，将移位寄 存器内容装载到锁存器。该器件结合了HVCMOS技术、双极性型DMOS开关和低功耗CMOS逻辑对高压模拟信号进行控制 。

该芯片适用于各种高电压电源，例如，Vpp/Vnn+60V/-60V.

应用：

- ▶医疗超声影像
- ▶无损探伤
- ▶压电传感器驱动
- ▶光学MEMS模组

方框图：



订购信息：

芯片型号	封装选择
	48-Lead LQPF 7.00x7.00mm body 1.60mm height (max) 0.50mm pitch
SY2160	SY2160FG

极限范围：

Parameter	Value
V_{DD} logic supply	-0.5V to +7.0V
V_{PP}-V_{NN} differential supply	140V
V_{PP} positive supply	-0.5V to V_{NN}+140V
V_{NN} negative supply	+0.5V to -70V
Logic input voltage	-0.5V to V_{DD} +0.3V
Analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	2.0A
Storage temperature	-65°C to 150°C
Power dissipation: 48-Lead LQFP (A)	1.0W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

建议工作条件：

Sym	Parameter	Value
V_{DD}	Logic power supply voltage	3.0V to 5.5V
V_{PP}	Positive high voltage supply	+40V to V_{NN} +120V
V_{NN}	Negative high voltage supply	-40V to -60V
V_{IH}	High level input voltage	0.9V_{DD} to V_{DD}
V_{IL}	Low level input voltage	0V to 0.1V_{DD}
V_{SIG}	Analog signal voltage peak-to-peak	V_{NN}+5V to V_{PP}-5V
T_A	Operating free air temperature	0°C to 70°C

Notes:

1. *Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.*
2. *V_{SIG} must be within V_{NN} and V_{PP} or floating during power up/down transition.*
3. *Rise and fall times of power supplies V_{DD}, V_{PP}, and V_{NN} should not be less than 1.0msec.*

DC Electrical Characteristics

(over recommended operating conditions unless otherwise noted)

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions	
		Min	Max	Min	Typ	Max	Min	Max			
R_{ONS}	Small signal switch ON-resistance	-	-	-	-	-	-	-	Ω		
		-	-	-	-	-	-	-			
		-	-	-	25	-	-	-		I_{SIG} = 5.0mA	V_{PP} = +60V, V_{NN} = -60V
		-	-	-	17	-	-	-		I_{SIG} = 200mA	
		-	-	-	-	-	-	-			
		-	-	-	-	-	-	-			
ΔR_{ONS}	Small signal switch ON-resistance matching	-	20	-	5.0	20	-	20	%	I_{SIG} = 5.0mA, V_{PP} = +60V, V_{NN} = -60V	
R_{ONL}	Large signal switch ON-resistance	-	-	-	35	-	-	-	Ω	V_{SIG}= V_{PP} -10V, I_{SIG} = 1.0A	
R_{INT}	Value of output bleed resistor	-	-	20	35	50	-	-	kΩ	Output Switch to RGND I_{RINT} = 0.5mA	
I_{SOL}	Switch OFF leakage per switch*	-	5.0	-	1.0	10	-	15	µA	V_{SIG} = V_{PP} -10V and V_{NN} +10V	
V_{OS}	DC offset switch OFF*	-	300	-	100	300	-	300	mV	No Load	
	DC offset switch ON*	-	500	-	100	500	-	500	mV		
I_{PPQ}	Quiescent V_{PP} supply current	-	-	-	1.4	-	-	-	µA	All switches OFF	
I_{NNQ}	Quiescent V_{NN} supply current	-	-	-	-1.6	-	-	-	µA	All switches OFF	
I_{PPQ}	Quiescent V_{PP} supply current	-	-	-	1.3	-	-	-	µA	All switches ON, I_{SW} = 5.0mA	
I_{NNQ}	Quiescent V_{NN} supply current	-	-	-	-1.5	-	-	-	µA	All switches ON, I_{SW} = 5.0mA	
I_{SW}	Switch output peak current	-	2.0	-	2.0	2.0	-	2.0	A	V_{SIG} duty cycle < 0.1%	
f_{SW}	Output switching frequency	-	-	-	-	50	-	-	kHz	Duty cycle = 50%	
I_{PP}	Average V_{PP} supply current	-	-	-	-	-	-	-	mA		All output switches are turning ON and OFF at 50kHz with no load.
		-	3.0	-	-	3.5	-	-		V_{PP} = +60V, V_{NN} = -60V	
		-	-	-	-	-	-	-			
I_{NN}	Average V_{NN} supply current	-	-	-	-	-	-	-	mA		All output switches are turning ON and OFF at 50kHz with no load.
		-	2.5	-	-	3.0	-	4.0		V_{PP} = +60V, V_{NN} = -60V	
		-	-	-	-	-	-	-			
I_{DD}	Average V_{DD} supply current	-	4.0	-	-	4.0	-	4.0	mA	f_{CLK} = 5.0MHz, V_{DD} = 10.0V	
I_{DDQ}	Quiescent V_{DD} supply current	-	1.0	-	-	1.0	-	1.0	µA	All logic inputs are static	
I_{SOR}	Data out source current	0.45	-	0.45	0.70	-	0.40	-	mA	V_{OUT} = V_{DD} - 0.7V	
I_{SINK}	Data out sink current	0.45	-	0.45	0.70	-	0.40	-	mA	V_{OUT} = 0.7V	
C_{IN}	Logic input capacitance	-	10	-	-	10	-	10	pF	---	

** See Test Circuits on page 5*

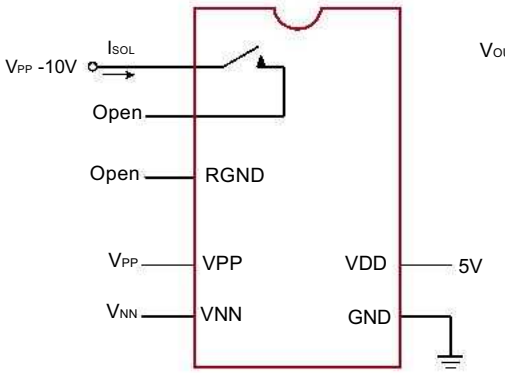
AC Electrical Characteristics

(over recommended operating conditions, V_{DD}= 5.0V, $t_R = t_F \leq$ 5.0ns, 50% duty cycle, C

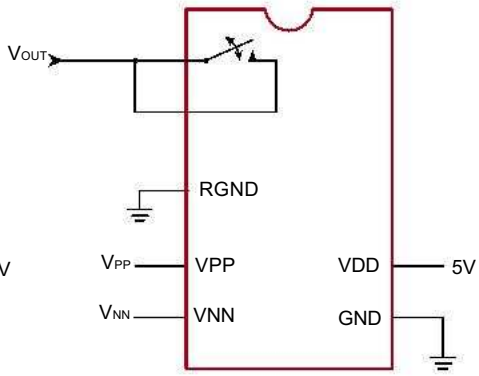
Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
t_{SD}	Set up time before $\overline{LE}$ rises	25	-	25	-	-	25	-	ns	---
t_{WLE}	Time width of $\overline{LE}$	56	-	-	56	-	56	-	ns	V_{DD} = 3.0V
		12	-	-	12	-	12	-		V_{DD} = 5.0V
t_{DO}	Clock delay time to data out	50	100	50	78	100	50	100	ns	V_{DD} = 3.0V
		15	40	15	30	40	15	40		V_{DD} = 5.0V
t_{WCLR}	Time width of CLR	55	-	55	-	-	55	-	ns	---
t_{SU}	Set up time data to clock	21	-	-	21	-	21	-	ns	V_{DD} = 3.0V
		7.0	-	-	7.0	-	7.0	-		V_{DD} = 5.0V
t_H	Hold time data from clock	2.0	-	2.0	-	-	2.0	-	ns	V_{DD} = 3.0 or 5.0V
f_{CLK}	Clock frequency	-	8.0	-	-	8.0	-	8.0	MHz	V_{DD} = 3.0V
		-	20	-	-	20	-	20		V_{DD} = 5.0V
t_R,t_F	Clock rise and fall times	-	50	-	-	50	-	50	ns	----
T_{ON}	Turn ON time*	-	0.2	-	-	0.2	-	0.2	µs	V_{SIG} = V_{PP} -10V, R_{LOAD} = 10kΩ
T_{OFF}	Turn OFF time*	-	0.5	-	-	0.5	-	0.5	µs	V_{SIG} = V_{PP} -10V, R_{LOAD} = 10kΩ
dv/dt	Maximum V_{SIG} slew rate	-	-	-	-	-	-	-	v/ns	
		-	20	-	-	20	-	20		V_{PP} = +60V, V_{NN} = -60V
		-	-	-	-	-	-	-		
K_O	OFF isolation*	-35	-	-	-35	-	-35	-	dB	f = 5.0MHz, 1.0kΩ//15pF load
		-56	-	-	-56	-	-56	-		f = 5.0MHz, 50Ω load
K_{CR}	Switch crosstalk*	-60	-	-	-60	-	-60	-	dB	f = 5.0MHz, 50Ω load
I_{ID}	Output switch isolation diode current	-	300	-	-	300	-	300	mA	300ns pulse width, 2.0% duty cycle
$C_{SG(OFF)}$	OFF capacitance SW to GND	5.0	17	5.0	12	17	5.0	17	pF	0V, f = 1.0MHz
$C_{SG(ON)}$	ON capacitance SW to GND	25	50	25	38	50	25	50	pF	0V, f = 1.0MHz
$+V_{SPK}$	Output voltage spike*	-	-	-	-	-	-	-	mV	
$-V_{SPK}$										
$+V_{SPK}$		-	-	-	-	150	-	-		V_{PP} = +60V, V_{NN} = -60V, R_{LOAD} = 50Ω
$-V_{SPK}$										
$+V_{SPK}$		-	-	-	-	-	-	-		
$-V_{SPK}$										
QC	Charge injection*	-	-	-	-	-	-	-	pC	
		-	-	-	600	-	-	-		V_{PP} = +60V, V_{NN} = -60V, V_{SIG} = 0V
		-	-	-	-	-	-	-		

** See Test Circuits on page 5*

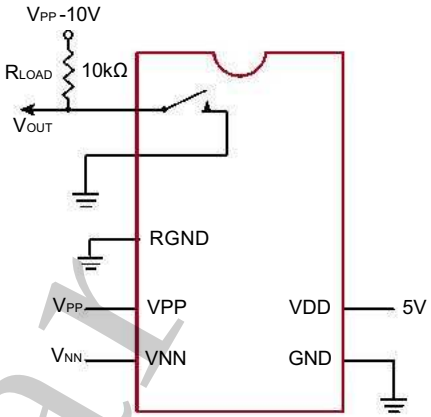
SY2160 Test Circuits



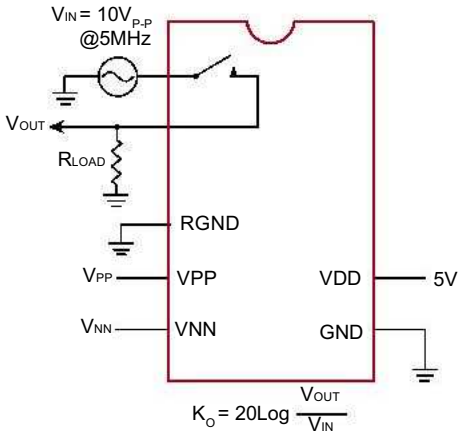
Switch Off Leakage per Switch



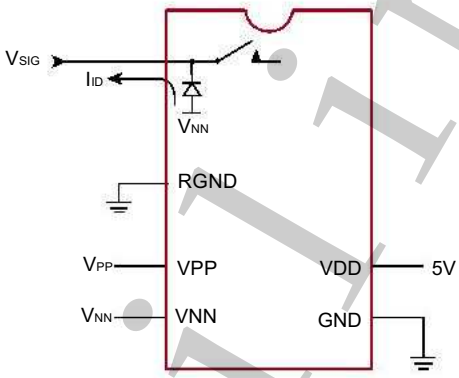
DC Offset Switch ON/OFF



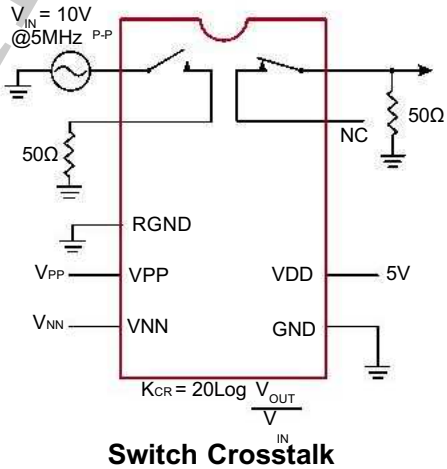
T /T Test Circuit
ON OFF



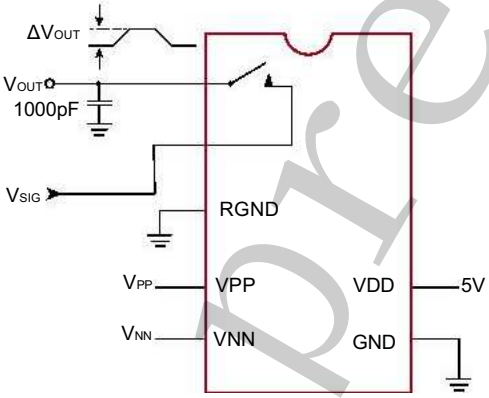
OFF Isolation



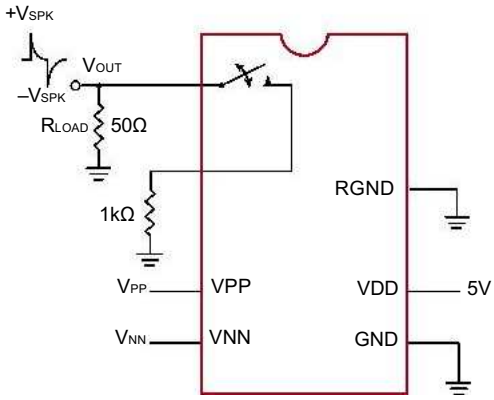
Output Switch Isolation Diode Current



Switch Crosstalk



Q = 1000pF x ΔV_{OUT}
Charge Injection



Output Voltage Spike

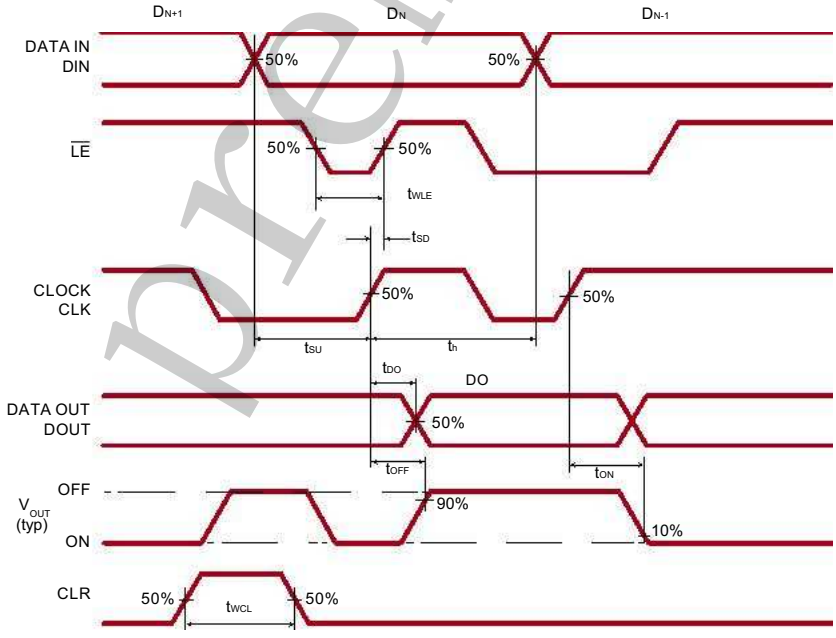
Logic Function Table

D0	D1	...	D7	D8	...	D15	$\overline{LE}$	CLR	SW0	SW1	...	SW7	SW8	...	SW15
L	-		-	-		-	L	L	OFF	-		-	-		-
H	-		-	-		-	L	L	ON	-		-	-		-
-	L		-	-		-	L	L	-	OFF		-	-		-
-	H		-	-		-	L	L	-	ON		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		L	-		-	L	L	-	-		OFF	-		-
-	-		H	-		-	L	L	-	-		ON	-		-
-	-	...	-	L	...	-	L	L	-	-	...	-	OFF	...	-
-	-		-	H		-	L	L	-	-		-	ON		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		L	L	L	-	-		-	-		OFF
-	-		-	-		H	L	L	-	-		-	-		ON
X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE						
X	X	X	X	X	X	X	X	H	ALL SWITCHES OFF						

Notes:

1. *The 16 switches operate independently.*
2. *Serial data is clocked in on the L to H transition of the CLK.*
3. *All 16 switches go to a state retaining their latched condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low the shift registers data flow through the latch.*
4. *D_{OUT} is high when data in the shift register 15 is high.*
5. *Shift registers clocking has no effect on the switch states if $\overline{LE}$ is high.*
6. *The CLR clear input overrides all other inputs.*

Logic Timing Waveforms

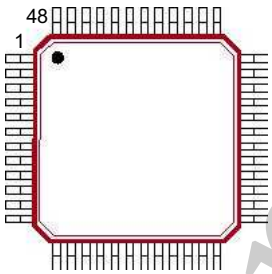


Pin Description

48-Lead LQFP (FG)

Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	NC	13	VNN	25	SW15B	37	SW10B
2	NC	14	NC	26	SW15A	38	SW10A
3	SW4B	15	VPP	27	SW14B	39	SW9B
4	SW4A	16	NC	28	SW14A	40	SW9A
5	SW3B	17	GND	29	SW13B	41	SW8B
6	SW3A	18	VDD	30	SW13A	42	SW8A
7	SW2B	19	DIN	31	SW12B	43	SW7B
8	SW2A	20	CLK	32	SW12A	44	SW7A
9	SW1B	21	$\overline{LE}$	33	SW11B	45	SW6B
10	SW1A	22	CLR	34	SW11A	46	SW6A
11	SW0B	23	DOUT	35	NC	47	SW5B
12	SW0A	24	RGND	36	NC	48	SW5A

Pin Configurations：



48-Lead LQFP (FG)

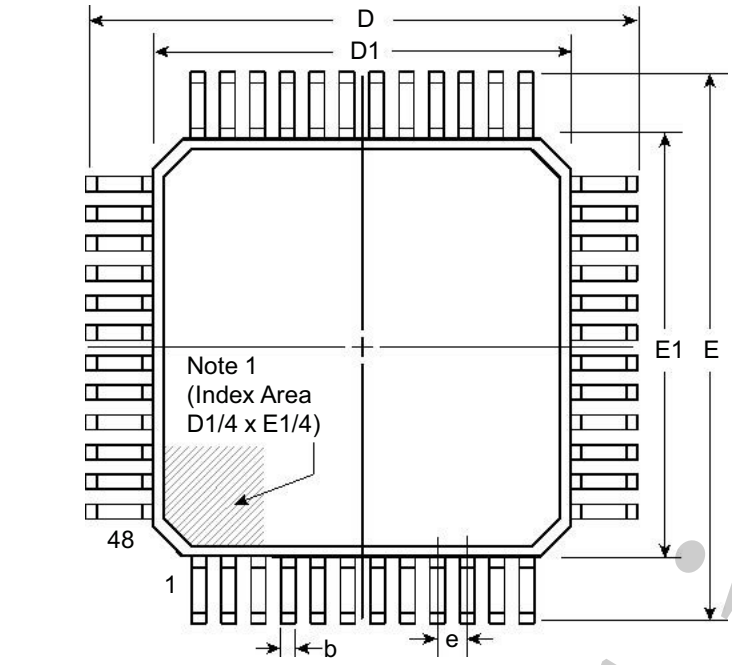
(top view)

Product Marking：

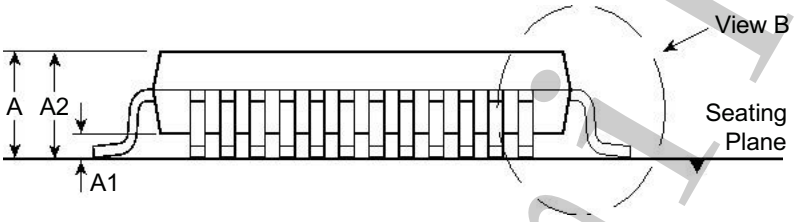
YY = Year Sealed
WW = Week Sealed
L = Lot Number

48-Lead LQFP Package Outline (FG)

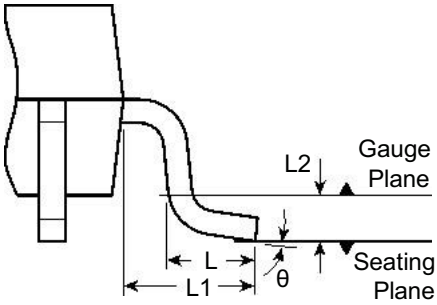
7.00x7.00mm body, 1.60mm height (max), 0.50mm pitch



Top View



Side View



View B

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ
Dimension (mm)	MIN	1.40*	0.05	1.35	0.17	8.80*	6.80*	8.80*	6.80*	0.50 BSC	0.45	1.00 REF	0.25 BSC	0°
	NOM	-	-	1.40	0.22	9.00	7.00	9.00	7.00		0.60			3.5°
	MAX	1.60	0.15	1.45	0.27	9.20*	7.20*	9.20*	7.20*		0.75			7°