低电荷注入、16通道、带泄放电阻高压模拟开关

特性：

- 0V至±100V模拟信号电压范围
- 无需正负高压供电，仅+5V供电
- 输出集成40KΩ泄放电阻
- 16通道高压模拟开关
- 50兆赫兹数据移位时钟频率
- 5V CMOS逻辑接口
- 非常低的静态功耗（10mW）
- 5.0MHz时的典型关断隔离度为-57dB
- 极低的开关串扰-60dB
- 低寄生电容
- 具有过温保护功能

应用：

- 医疗超声影像
- 无损探伤
- 压电传感器驱动
- 光学MEMS模组

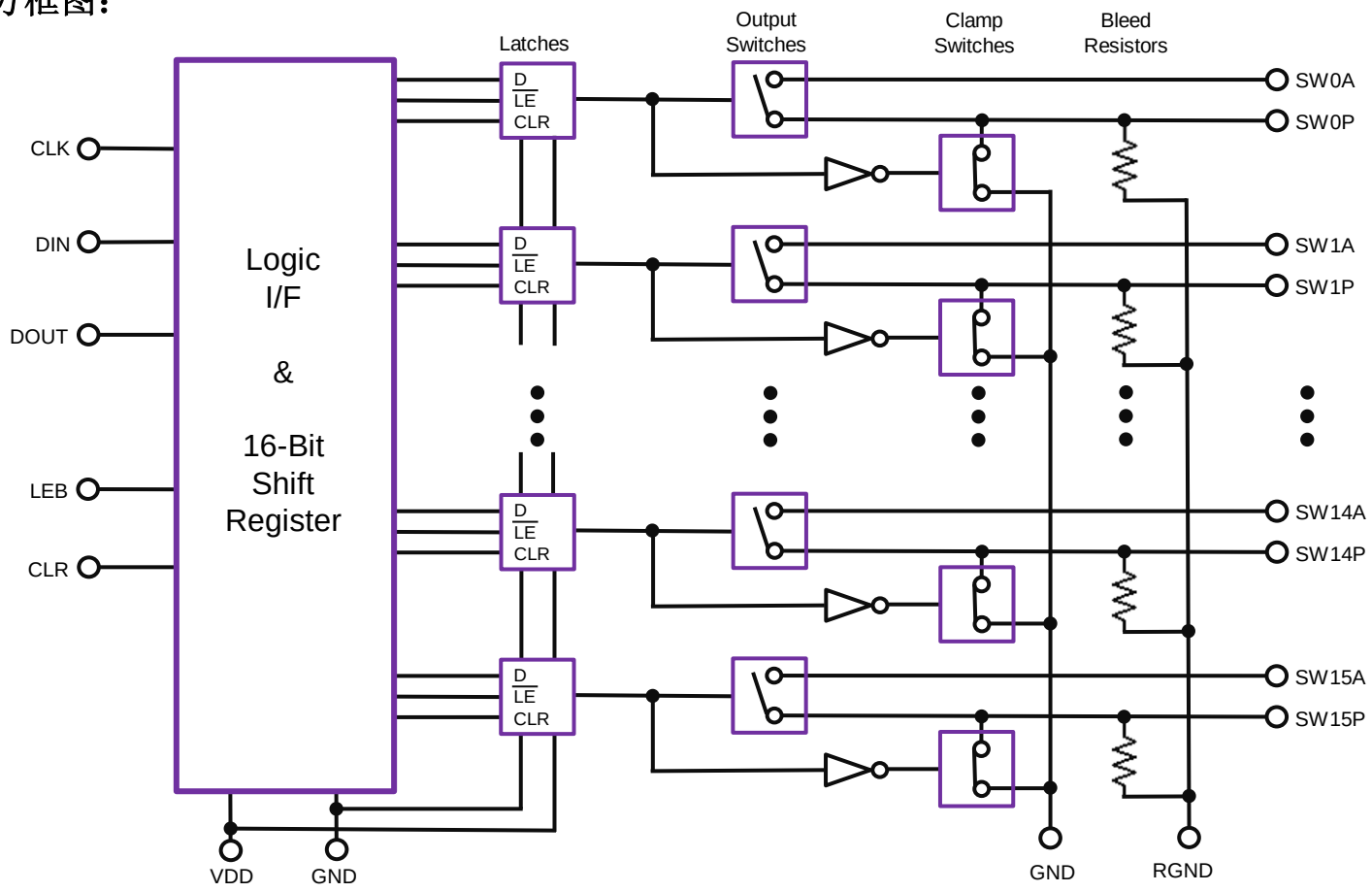
概述：

SY2162为一款低电荷注入，16通道，高压模拟开关集成电路。这芯片是为以下应用而设计的需要低压信号控制的高压开关，如医学超声图像、工业无损探伤和其他压电传感器驱动器。 SY2162集成了泄放电阻，用来消除电容性负载（如压电传感器）两端积累噪声电压。

该器件将输入数据移位到16位移位寄存器中，然后可以保留在16位锁存器中。为了减少时钟馈通引入的噪声，在数据载入移位寄存器期间将LEB拉至高电平。当移位寄存器装载有效数据后，在LEB作用一个低电平脉冲，将移位寄存器内容装载到锁存器。该器件结合了HVCMOS技术、双极性型DMOS开关和低功耗CMOS逻辑对高压模拟信号进行控制 。

该芯片仅需要+5V电源供电，不需要正负高压供电。

方框图：



器件SWxA脚接AFE侧，SWxP脚接Probe侧。

1，订购信息：

芯片型号	封装 48-LQFP 7.00x7.00mm body 1.6mm height (max) 0.50mm pitch
SY2162	SY2162QF

2，极限范围：

T_A=25℃, unless otherwise specified

No	Items	Symbol	Typ	Units	Condition
1	Positive supply voltage	V_{DD}	-0.4 to +7	V	
2	Logic input voltage	DIN, LEB, CLK, CLR	-0.4 to +7	V	
3	Logic output voltage	D_{OUT}	-0.4 to +7	V	
4	Analog signal range	V_{SIG}	-105 to +105	V	
5	Peak analog signal current per channel	I_{SW}	2.0	A	
6	Operating junction temperature	T_{Jop}	-20 to +150	℃	
7	Storage temperature	T_{STG}	-55 to +150	℃	
8	Maximum power dissipation	P_{Dmax}	1	W	

3，建议工作条件：

No.	Items	Symbol	Min	Typ	Max	Units	Condition
1	Positive supply voltage	V_{DD}	4.75	5	5.25	V	
2	IC substrate voltage	V_{SUB}	-	0	-	V	
3	Operating free-air temperature	T_A	0		75	℃	
4	High-level logic input voltage	V_{IH}	0.8V_{DD}	-	V_{DD}	V	
5	Low-level logic input voltage	V_{IL}	0	-	0.2V_{DD}	V	
6	Logic input high current	I_{IH}	-10	-	10	pA	DIN, LEB, CLK, CLR
7	Logic input low current	I_{IL}	-10	-	10	pA	
8	Logic input capacitance	C_{IN}	-	2	-	pF	
9	Setup time before LEB rises	t_{SD}	25	-	-	ns	
10	Time width of LEB	t_{WLEB}	12	-	-	ns	
11	Clock delay time to data out	t_{DO}	7	10	-	ns	
12	Time width of CLR	t_{WCLR}	55	-	-	ns	
13	Clock frequency	f_{CLK}	-	-	50	MHz	
14	Clock rise and fall times	t_R, t_F	-	-	50	ns	
15	Setup time data to clock	t_{SU}	7	-	-	ns	
16	Hold time data from clock	t_{HLD}	7	-	-	ns	

4， DC Electrical Characteristics

V_{DD}=5V, LEB=0, T_A=25 ℃, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Analog signal range	V_{SIG}	-100	-	100	V	
2	V_{DD} quiescent current	I_{DDQ}	-	1	-	mA	All main switches off
3	V_{DD} quiescent current	I_{DDQ}	-	1		mA	All main switches on
4	V_{DD} dynamic current	I_{DD}	-	2.8	3.8	mA	Dynamic current All channels switching simultaneously at f_{SW}=50kHz
5	DC offset main switch off	V_{OS}	-	0	-	mV	No load
6	Small signal main switch on-resistance	R_{ONS}	-	8	10	Ω	V_{SIG}=0.1Vpp to 5Vpp @5MHz, R_S=10Ω
7	Small signal main switch on-resistance matching	ΔR_{ONS}	-	2	5	%	V_{SIG}=0V, I_{SIG}=5mA
8	Large signal main switch on-resistance	R_{ONL}	-	8	-	Ω	V_{SIG}=20Vpp @5MHz, R_S=10Ω
9	GND clamp on-resistance	R_{ONCL}	-	35	-	Ω	Main switches off, probe side
10	Shunt resistance	R_{BLD}	30	40	50	kΩ	Probe side
11	Switch output peak current	I_{SW}	-	2	-	A	100ns pulse, 0.1% duty cycle

5， Thermal Protection

V_{DD}=5V, LEB=0, T_A=25 ℃, unless otherwise specified

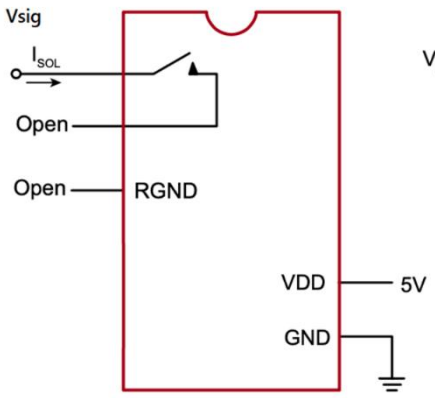
No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	THP temperature threshold	T_{THP}	90	110	130	℃	
2	THP reset hysteresis	T_{HYSTHP}	-	10	-	℃	

6， AC Characteristics

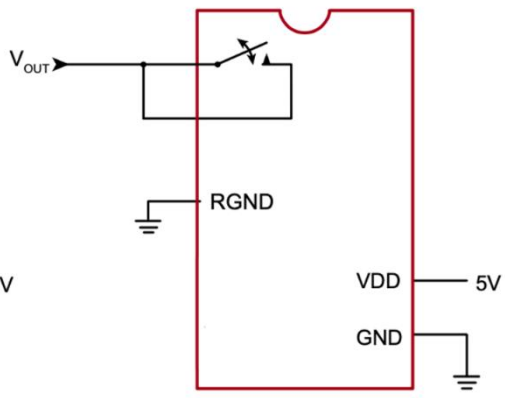
V_{DD}=5V, LEB=0, , T_A=25 ℃, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Turn-on time	t_{ON}	-	2	5	us	
2	Turn-off time	t_{OFF}	-	2	5	us	
3	Output switching frequency	f_{SW}	-	-	50	kHz	Duty cycle=50%
4	Small signal frequency	f_{SIG}	0.01	-	20	MHz	C_L=220pF
5	Off isolation	V_O	-	-53	-	dB	f_{SIG}=5MHz, R_L//C_L=1kΩ//15pF
			-	-57	-	dB	f_{SIG}=5MHz, R_L=50Ω
6	Crosstalk	V_{CR}	-	-60	-	dB	f_{SIG}=5MHz, R_L=50Ω
7	Off capacitance SWxP to GND	$C_{OFF(SWxP)}$	-	22	-	pF	V_{SIG}=0V, f_{SIG}=1MHz
8	Off capacitance SWxA to GND	$C_{OFF(SWxA)}$	-	60	-	pF	V_{SIG}=0V, f_{SIG}=1MHz
9	On capacitance SWxP to GND	$C_{ON(SWxP)}$	-	45	-	pF	V_{SIG}=0V, f_{SIG}=1MHz
10	On capacitance SWxA to GND	$C_{ON(SWxA)}$	-	45	-	pF	V_{SIG}=0V, f_{SIG}=1MHz
11	Output spike voltage (SWxP)	$V_{SPK\_ON\ (SWxP)}$	-15	40	60	mV	50Ω load @switch on
		$V_{SPK\_OFF\ (SWxP)}$	-15	60	90	mV	50Ω load @switch off
12	Output spike voltage (SWxA)	$V_{SPK\_ON\ (SWxA)}$	-15	40	60	mV	50Ω load @switch on
		$V_{SPK\_OFF(SWxA)}$	-15	60	90	mV	50Ω load @switch off
13	Charge injection (per switch)	QC	-	10	-	pC	

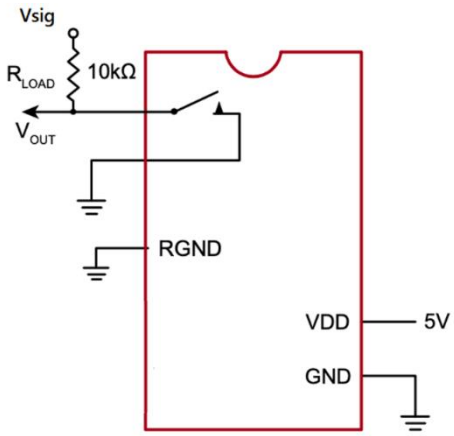
7， SY2162 Test Circuits



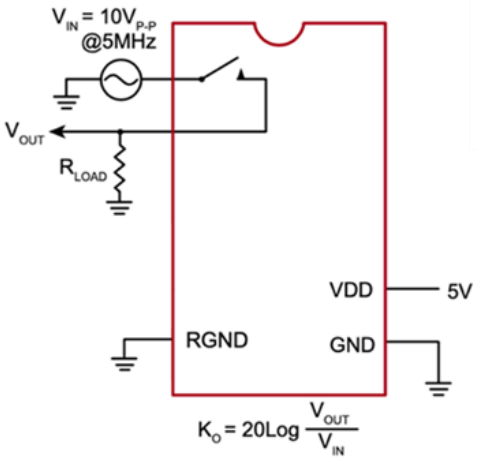
Switch Off Leakage per Switch



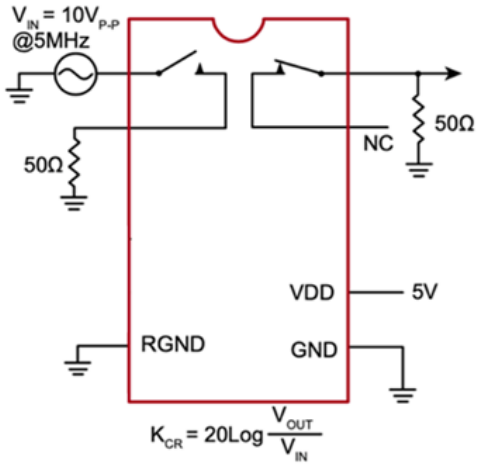
DC Offset Switch ON/OFF



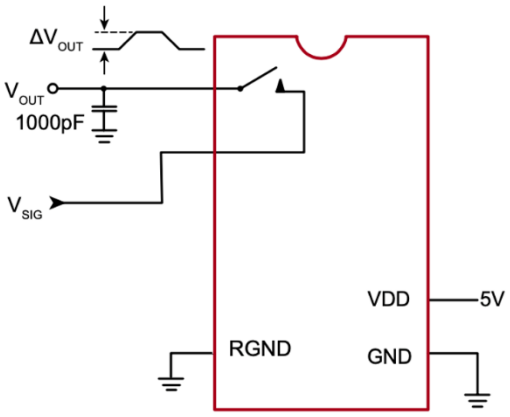
T_{ON}/T_{OFF} Test Circuit



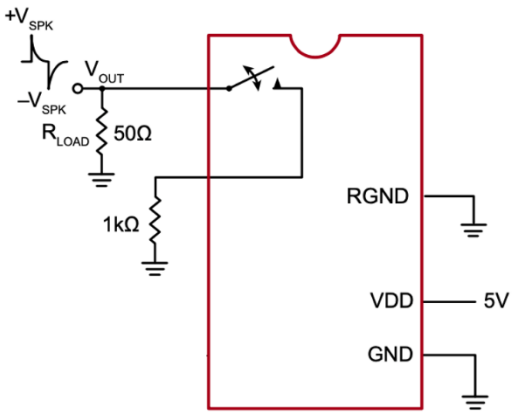
OFF Isolation



Switch Crosstalk



Q = 1000pF x ΔV_{OUT} Charge Injection



Output Voltage Spike

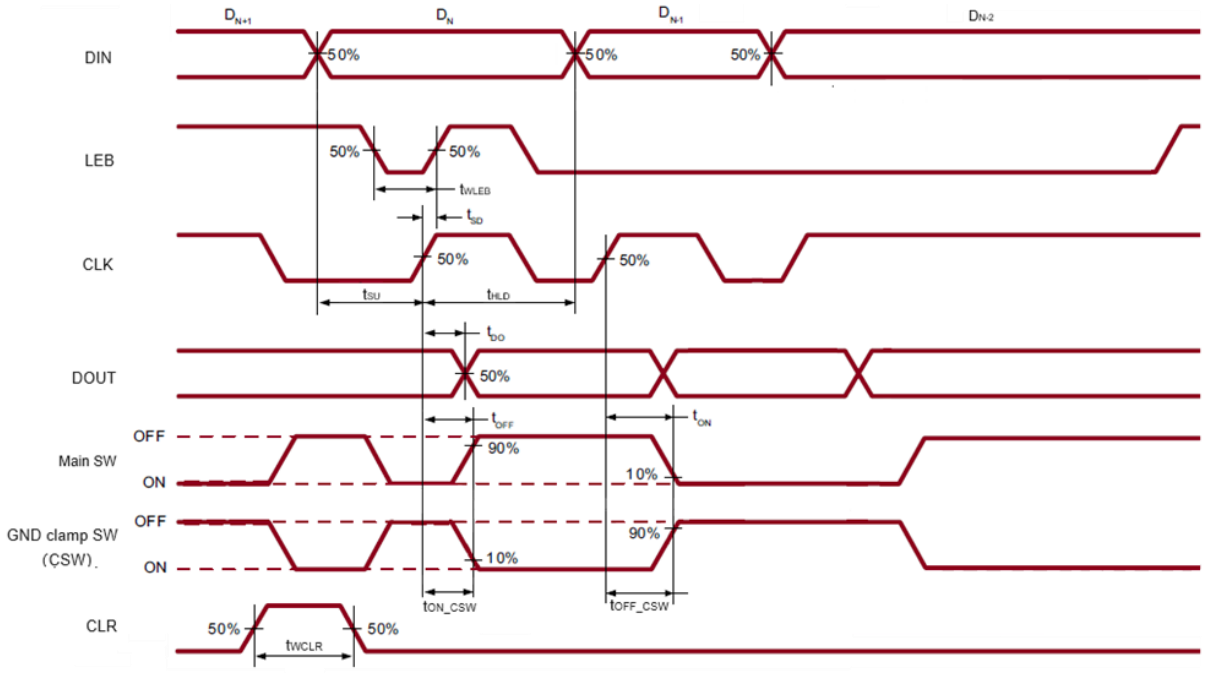
8， Logic Function Table

Logic Inputs									Analog Switch State											
LEB	CLR	DIN							SW0		SW1		...	SW7		SW8		...	SW15	
		D0	D1	...	D17	D18	...	D15	Main SW	Clamp SW	Main SW	Clamp SW	...	Main SW	Clamp SW	Main SW	Clamp SW	...	Main SW	Clamp SW
L	L	L	-		-	-		-	OFF	ON	-	-		-	-	-	-		-	-
L	L	H	-		-	-		-	ON	OFF	-	-		-	-	-	-		-	-
L	L	-	L		-	-		-	-	-	OFF	ON		-	-	-	-		-	-
L	L	-	H		-	-		-	-	-	ON	OFF		-	-	-	-		-	-
L	L	-	-		-	-		-	-	-	-	-		-	-	-	-		-	-
L	L	-	-		-	-		-	-	-	-	-		-	-	-	-		-	-
L	L	-	-		L	-		-	-	-	-	-		OFF	ON	-	-		-	-
L	L	-	-		H	-		-	-	-	-	-		ON	OFF	-	-		-	-
L	L	-	-	...	-	L	...	-	-	-	-	-	...	-	-	OFF	ON	...	-	-
L	L	-	-		-	H		-	-	-	-	-		-	-	ON	OFF		-	-
L	L	-	-		-	-		-	-	-	-	-		-	-	-	-		-	-
L	L	-	-		-	-		-	-	-	-	-		-	-	-	-		-	-
L	L	-	-		-	-		-	-	-	-	-		-	-	-	-		-	-
L	L	-	-		-	-		-	-	-	-	-		-	-	-	-		-	-
L	L	-	-		-	-		L	-	-	-	-		-	-	-	-		OFF	ON
L	L	-	-		-	-		H	-	-	-	-		-	-	-	-		ON	OFF
H	L	X	X	X	X	X	X	X	Hold Previous State											
X	H	X	X	X	X	X	X	X	ALL "Main SWs" OFF											

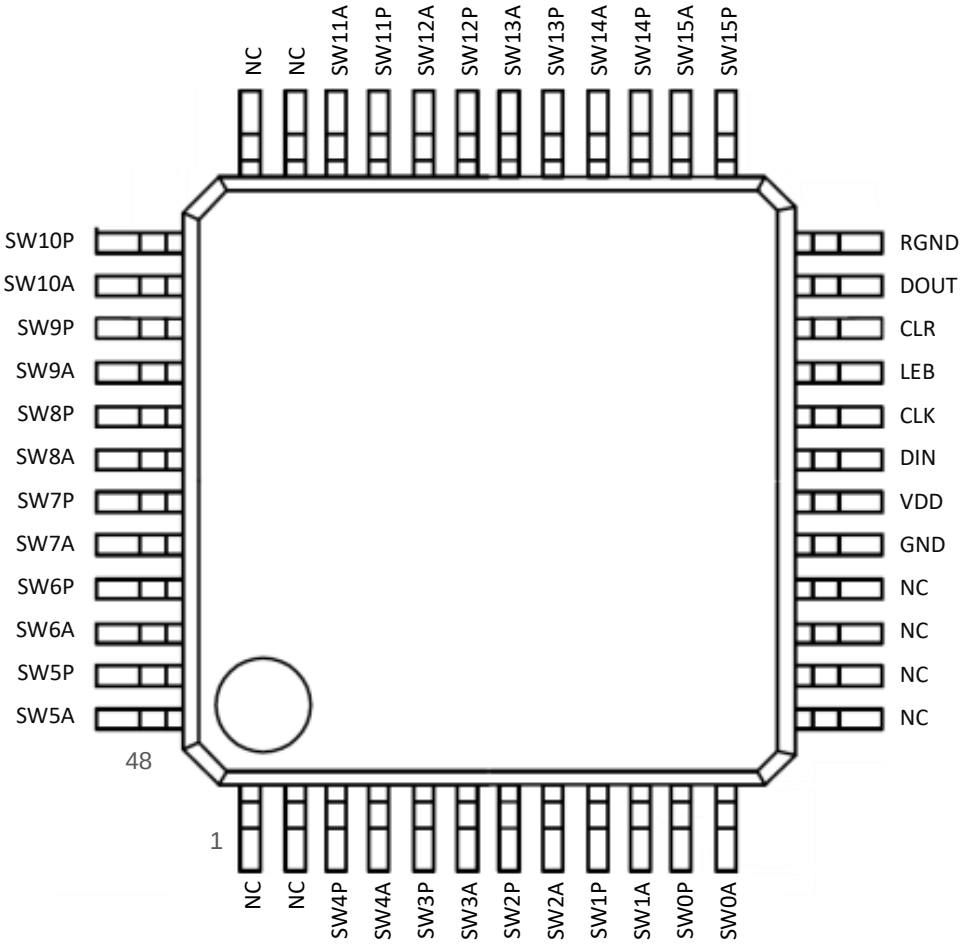
Notes:

1. The 16 switches operate independently.
2. Serial data is clocked in on the L to H transition of the CLK.
3. All 16 switches go to a state retaining their latched condition at the rising edge of LEB. When LEB is low the shift registers data flow through the latch.
4. Dout is high when data in the shift register 15 is high.
5. Shift registers clocking has no effect on the switch states if LEB is high.
6. The CLR clear input overrides all other inputs.

9， Logic Timing Waveforms

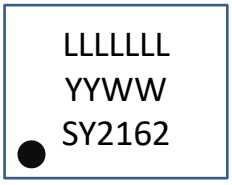


10， Pin Configuration



48-Lead LQFP

11， Product Marking：



48-Lead LQFP

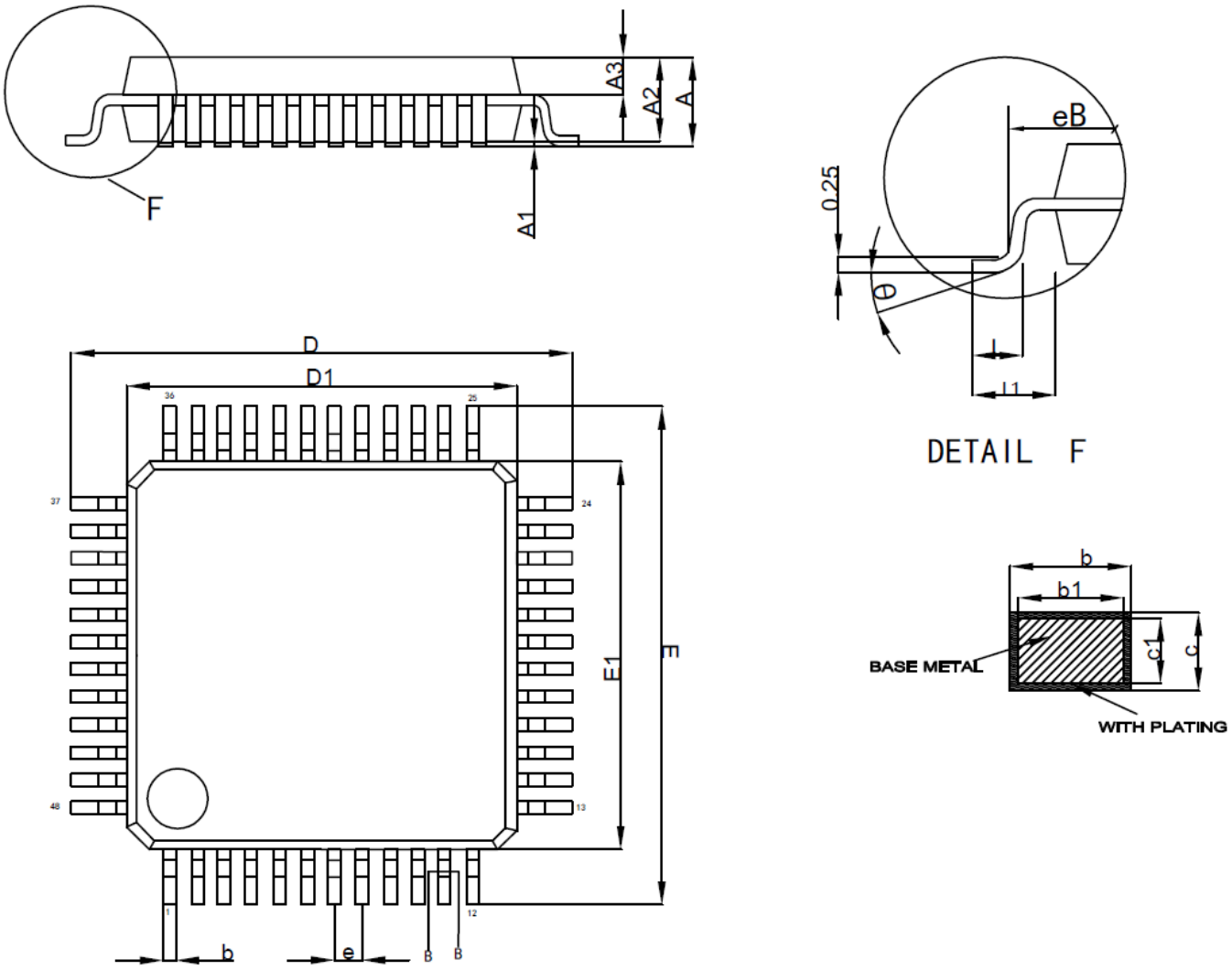
L = Lot Number
YY = Year Sealed
WW = Week Sealed

12， Pin Function

Pin#	Function	Pin#	Function	Pin#	Function	Pin#	Function
1	NC	13	NC	25	SW15P	37	SW10P
2	NC	14	NC	26	SW15A	38	SW10A
3	SW4P	15	NC	27	SW14P	39	SW9P
4	SW4A	16	NC	28	SW14A	40	SW9A
5	SW3P	17	GND	29	SW13P	41	SW8P
6	SW3A	18	VDD	30	SW13A	42	SW8A
7	SW2P	19	DIN	31	SW12P	43	SW7P
8	SW2A	20	CLK	32	SW12A	44	SW7A
9	SW1P	21	LEB	33	SW11P	45	SW6P
10	SW1A	22	CLR	34	SW11A	46	SW6A
11	SW0P	23	DOUT	35	NC	47	SW5P
12	SW0A	24	RGND	36	NC	48	SW5A

13， 48-Lead LQFP Package Outline

7.00x7.00mm body, 1.40mm height (max), 0.50mm pitch



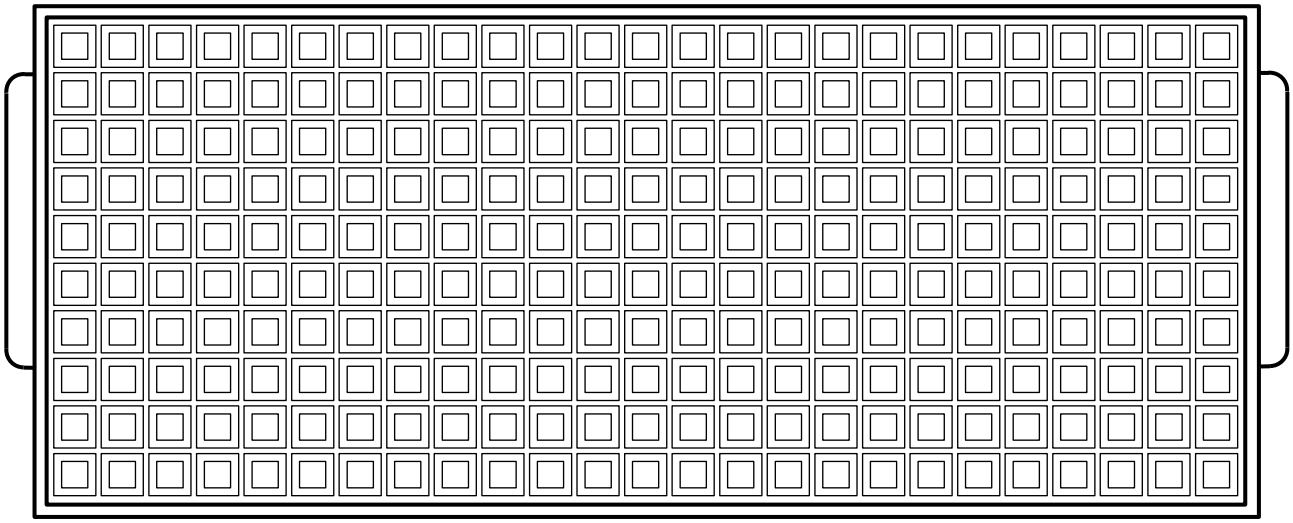
Note:

A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol		A	A1	A2	A3	b	c	c1	D	D1	E	E1	eB	e	L	L1	θ
Dimension (mm)	Min	1.40	0.05	1.35	0.60	0.18	0.13	0.12	8.80	6.90	8.80	6.90	8.10	0.50 BSC	0.40	1.00 REF	0°
	Nom	-	-	1.40	-	0.22	-	0.13	9.00	7.00	9.00	7.00	-		-		-
	Max	1.60	0.15	1.45	0.64	0.26	0.17	0.14	9.20	7.10	9.20	7.10	8.25		0.65		8°

14， Product Identification Information

PART NO. XX XX Device Package Media Type Device: SY2162: 16-Channel High Voltage Analog Switch Package: QF: LQFP Media Type: (blank): 2500pcs for MOQ	**Examples:** SY2162QF: 16-Channel High Voltage Analog Switch 48-lead LQFP, 7.00x7.00mm body 250/Tray x10 for MOQ



Revision History

Revision #	Revision Date	Pages Updated	Description
Rev. 0.0	2023-07-19		Initially released
Rev. 0.1	2023-09-02		Changed clock frequency