低电荷注入、64通道、带泄放电阻高压模拟开关

特性：

- 0V至±100V模拟信号电压范围
- 无需正负高压供电，仅+5V供电
- 输出集成40KΩ泄放电阻
- 64通道高压模拟开关
- 50兆赫兹数据移位时钟频率
- 1.8V-5V CMOS逻辑接口
- 非常低的静态功耗（10mW）
- 5.0MHz时的典型关断隔离度为-57dB
- 极低的开关串扰度-60dB
- 低寄生电容

应用：

- 医疗超声影像
- 无损探伤
- 压电传感器驱动
- 光学MEMS模组

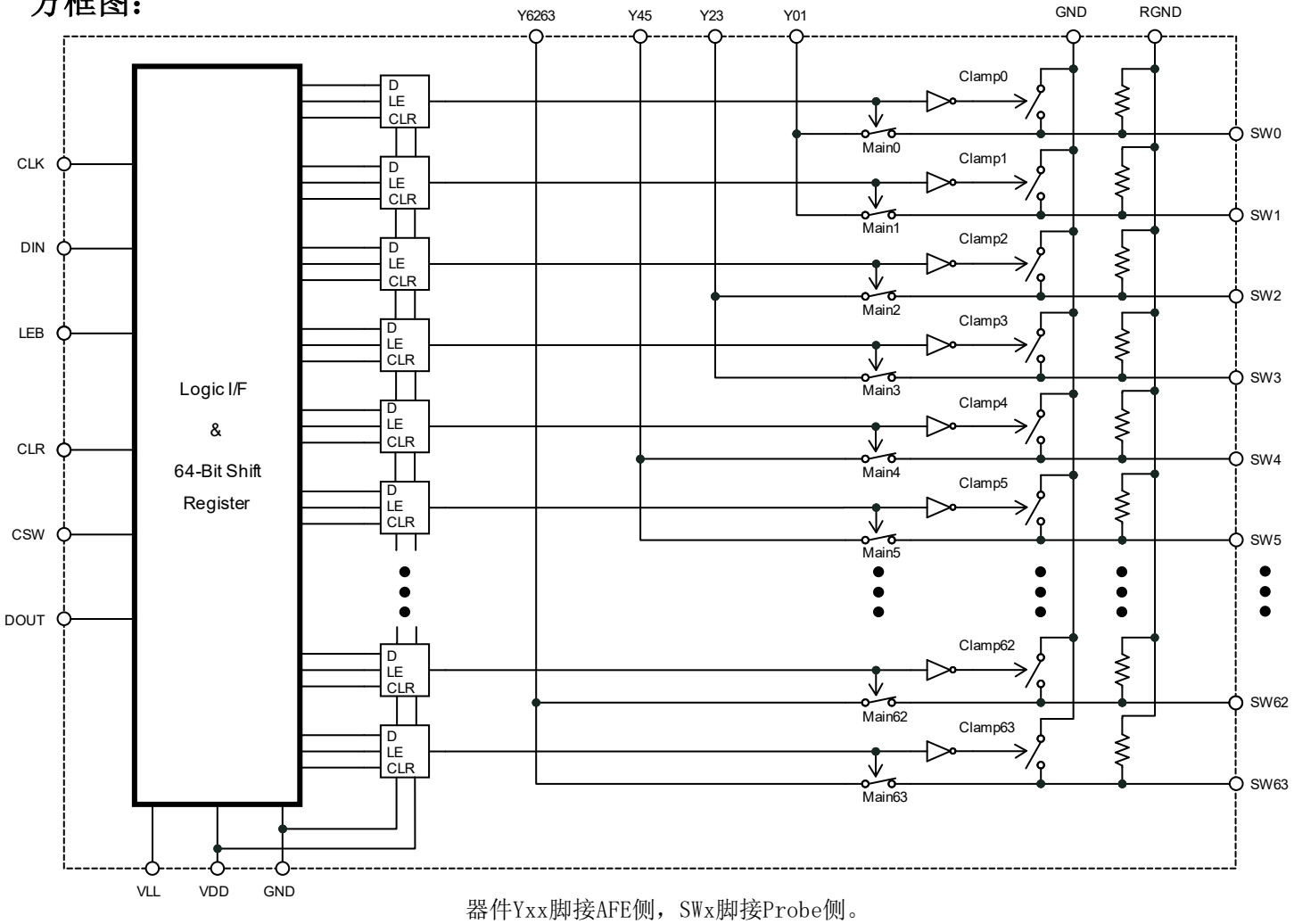
概述：

SY2642为一款低电荷注入，64通道， 1:2 MUX 高压模拟开关集成电路。这芯片是为以下应用而设计的需要低压信号控制的高压开关，如医学超声图像、工业无损探伤和其他压电传感器驱动器。 SY2642集成了泄放电阻，用来消除电容性负载（如压电传感器）两端积累噪声电压。

该器件将输入数据移位到64位移位寄存器中，然后可以保留在64位锁存器中。为了减少时钟馈通引入的噪声，在数据载入移位寄存器期间将LEB拉至高电平。当移位寄存器装载有效数据后，在LEB作用一个低电平脉冲，将移位寄存器内容装载到锁存器。该器件结合了HVCMOS技术、双极性型DMOS开关和低功耗CMOS逻辑对高压模拟信号进行控制 。

该芯片仅需要+5V电源供电，不需要正负高压供电。

方框图：



器件Yxx脚接AFE侧，SWx脚接Probe侧。

1，订购信息：

芯片型号	封装
	110-Lead LGA 14.50 x 10.00mm body 0.90mm height (max) 0.40mm pitch
SY2642	SY2642GA

2，极限范围：

T_A=25℃, unless otherwise specified

No	Items	Symbol	Typ	Units	Condition
1	Positive logic supply voltage	V_{LL}	-0.4 to +7	V	
2	Positive supply voltage	V_{DD}	-0.4 to +7	V	
3	Logic input voltage	DIN, LEB, CLK, CLR, CSW	-0.4 to +7	V	
4	Logic output voltage	D_{OUT}	-0.4 to +7	V	
5	Analog signal range	V_{SIG}	-105 to +105	V	
6	Peak analog signal current per channel	I_{SW}	2	A	
7	Operating junction temperature	T_{Jop}	-20 to +150	℃	
8	Storage temperature	T_{STG}	-55 to +150	℃	
9	Maximum power dissipation	P_{Dmax}	4	W	

3，建议工作条件：

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	Logic supply voltage	V_{LL}	1.7	1.8 to 5	V_{DD}	V	
2	Positive supply voltage	V_{DD}	4.75	5	5.25	V	
3	IC substrate voltage	V_{SUB}	-	0	-	V	
4	Operating free-air temperature	T_A	0		75	℃	
5	High-level logic input voltage	V_{IH}	0.8V_{LL}	-	V_{LL}	V	
6	Low-level logic input voltage	V_{IL}	0	-	0.2V_{LL}	V	
7	Logic input high current	I_{IH}	-10	-	10	pA	DIN, LEB, CLK, CLR, CSW
8	Logic input low current	I_{IL}	-10	-	10	pA	
9	Logic input capacitance	C_{IN}	-	2	-	pF	
10	Setup time before LEB rises	t_{SD}	25	-	-	ns	
11	Time width of LEB	t_{WLEB}	12	-	-	ns	
12	Clock delay time to data out	t_{DO}	7	10	-	ns	
13	Time width of CLR	t_{WCLR}	55	-	-	ns	
14	Clock frequency	f_{CLK}	-	-	50	MHz	
15	Clock rise and fall times	t_R, t_F	-	-	50	ns	
16	Setup time data to clock	t_{SU}	7	-	-	ns	
17	Hold time data from clock	t_{HLD}	7	-	-	ns	
18	Time width of CSW	t_{WCSW}	10	-	-	us	

4, DC Electrical Characteristics

V_{LL}=3.3V, V_{DD}=5V, LEB=0, CSW=0/1, T_A=25℃, unless otherwise specified.

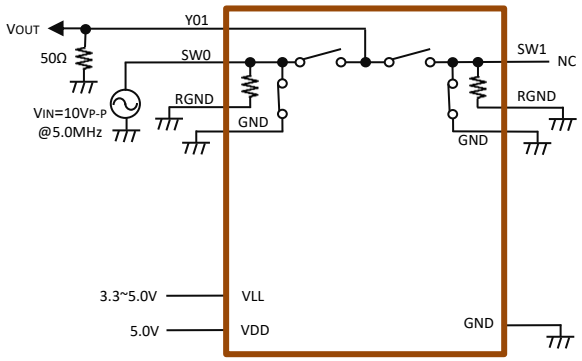
No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Analog signal range	V_{SIG}	-100	-	100	V	
2	V_{LL} quiescent current	I_{LLQ}	-	5	-	μA	Quiescent current-1
3	V_{DD} quiescent current	I_{DDQ}	-	1.2	-	mA	All main switches OFF
4	V_{LL} quiescent current	I_{LLQ}	-	5	-	μA	Quiescent current-2
5	V_{DD}quiescentcurrent	I_{DDQ}	-	1.2		mA	All main switches ON
6	V_{LL} dynamic current	I_{LL}	-	10	30	μA	Dynamic current All channels switching simultaneously
7	V_{DD} dynamic current	I_{DD}	-	2.8	3.8	mA	at f_{SW}=50kHz
8	DC offset main switch off	V_{OS}	-	0	-	mV	CSW=0
				0.8	10	mV	CSW=1
9	Small signal main switch on-resistance	R_{ONS}	-	8	10	Ω	V_{SIG}=0.1Vpp to 5Vpp @5MHz,R_S=10Ω
10	Small signal main switch on-resistance matching	ΔR_{ONS}	-	2	5	%	V_{SIG}=0V,I_{SIG}=5mA
11	Large signal main switch on-resistance	R_{ONL}	-	8	-	Ω	V_{SIG}=20Vpp@5MHz, R_S=10Ω
12	GND clamp on-resistance	R_{ONCL}	-	35	-	Ω	Main switches off, probe side
13	Output Bleed Resistor	R_{BLD}	30	40	50	kΩ	Probe side
14	Switch output peak current	I_{SW}	-	2	-	A	100ns pulse, 0.1% duty cycle

5, AC Characteristics

V_{LL}=3.3V, V_{DD}=5V, LEB=0, CSW=0/1, T_A=25 ℃, unless otherwise specified.

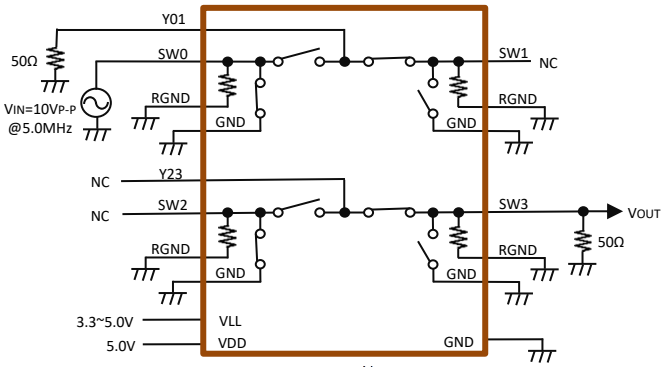
No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Turn-on time	t_{ON}	-	2	5	us	
		t_{ON_CSW}	-	2	5	us	
2	Turn-off time	t_{OFF}	-	2	5	us	
		t_{OFF_CSW}	-	2	5	us	
3	Output switching frequency	f_{SW}	-	-	50	KHz	Duty cycle=50%
4	Small signal frequency	f_{SIG}	0.01	-	20	MHz	CL=220pF
5	Off isolation	V_O	-	-53	-	dB	f_{SIG}=5MHz, R_L//C_L=1kΩ//15pF, CSW=0
			-	-57	-	dB	f_{SIG}=5MHz, R_L=50Ω, CSW=0
			-	-25	-	dB	f_{SIG}=5MHz, R_L//C_L=1kΩ//15pF, CSW=1
			-	-49	-	dB	f_{SIG}=5MHz, R_L=50Ω, CSW=1
6	Crosstalk	V_{CR}	-	-60	-	dB	f_{SIG}=5MHz, R_L=50Ω
7	Off capacitance SWx to GND (both SW OFF)	$C_{OFF(SW)}$	-	22	-	pF	V_{SIG}=0V, f_{SIG}=1MHz, CSW=0
			-	16	-	pF	V_{SIG}=0V, f_{SIG}=1MHz, CSW=1
8	Off capacitance Yxx to GND (both SW OFF)	$C_{OFF(Y)}$	-	60	-	pF	V_{SIG}=0V, f_{SIG}=1MHz, CSW=0
			-	20	-	pF	V_{SIG}=0V, f_{SIG}=1MHz, CSW=1
9	On capacitance SWx to GND (one SW ON, another SW OFF)	$C_{ON(SW)}$	-	45	-	pF	V_{SIG}=0V, f_{SIG}=1MHz, CSW=0
			-	30	-	pF	V_{SIG}=0V, f_{SIG}=1MHz, CSW=1
10	On capacitance Yxx to GND (one SW ON, another SW OFF)	$C_{ON(Y)}$	-	45	-	pF	V_{SIG}=0V, f_{SIG}=1MHz, CSW=0
			-	30	-	pF	V_{SIG}=0V, f_{SIG}=1MHz, CSW=1
11	Output spike voltage (SWx)	V_{SPK_ON} (SW)	-15	40	60	mV	50Ω load @switch on, CSW=0
			-15	80	120	mV	50Ω load @switch on, CSW=1
		V_{SPK_OFF} (SW)	-15	60	90	mV	50Ω load @switch off, CSW=0
			-15	100	150	mV	50Ω load @switch off, CSW=1
12	Output spike voltage (Yxx)	V_{SPK_ON} (Y)	-15	40	60	mV	50Ω load @switch on, CSW=0
			-15	80	120	mV	50Ω load @switch on, CSW=1
		V_{SPK_OFF} (Y)	-15	60	90	mV	50Ω load @switch off, CSW=0
			-15	100	150	mV	50Ω load @switch off, CSW=1
13	Charge injection (per switch)	QC	-	10	-	pC	

6, SY2642 Test Circuits



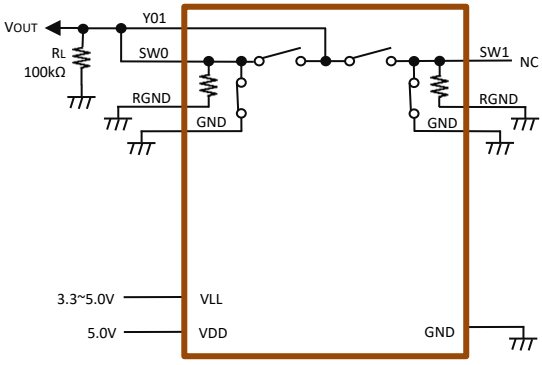
$K_O = 20Log\frac{V_{OUT}}{V_{IN}}$

Off isolation

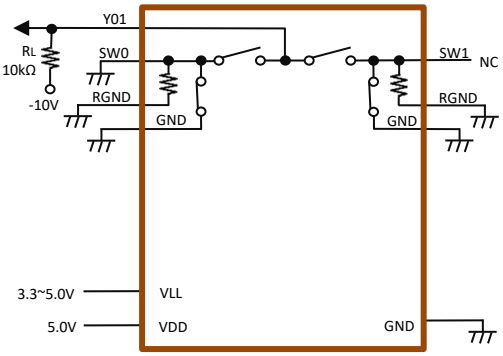


$K_{CR} = 20Log\frac{V_{OUT}}{V_{IN}}$

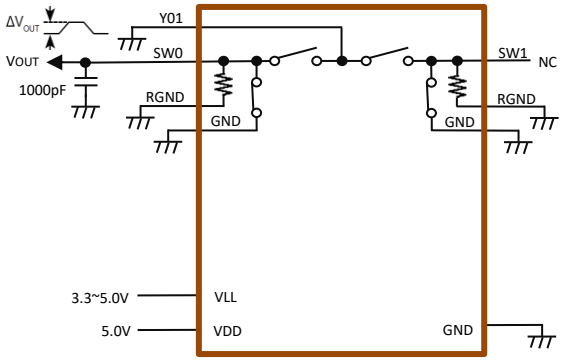
Crosstalk



DC Offset OFF

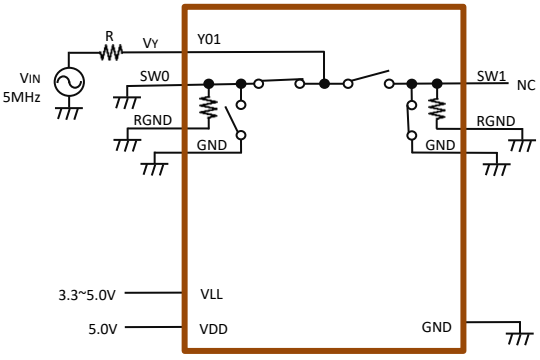


tON/tOFF Test Circuit



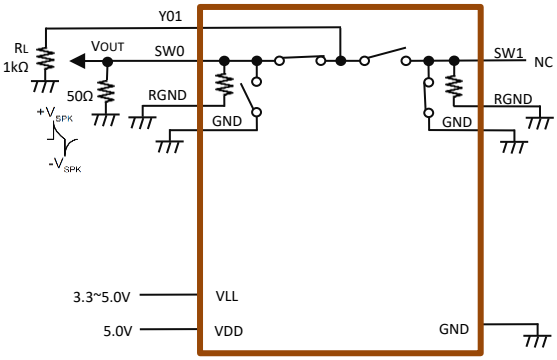
Q = 1000pF * ΔVOUT

Charge Injection

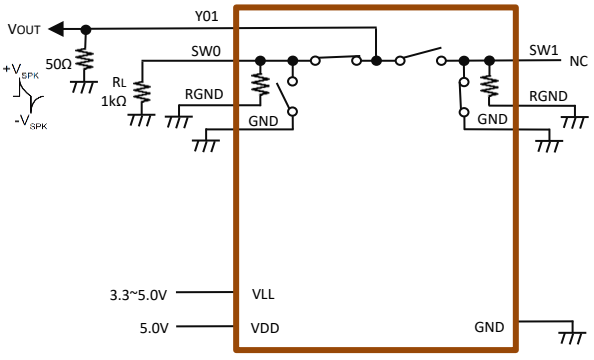


RON=R*VY/(VIN-VY)

On resistance test circuit



Output Voltage Spike SW

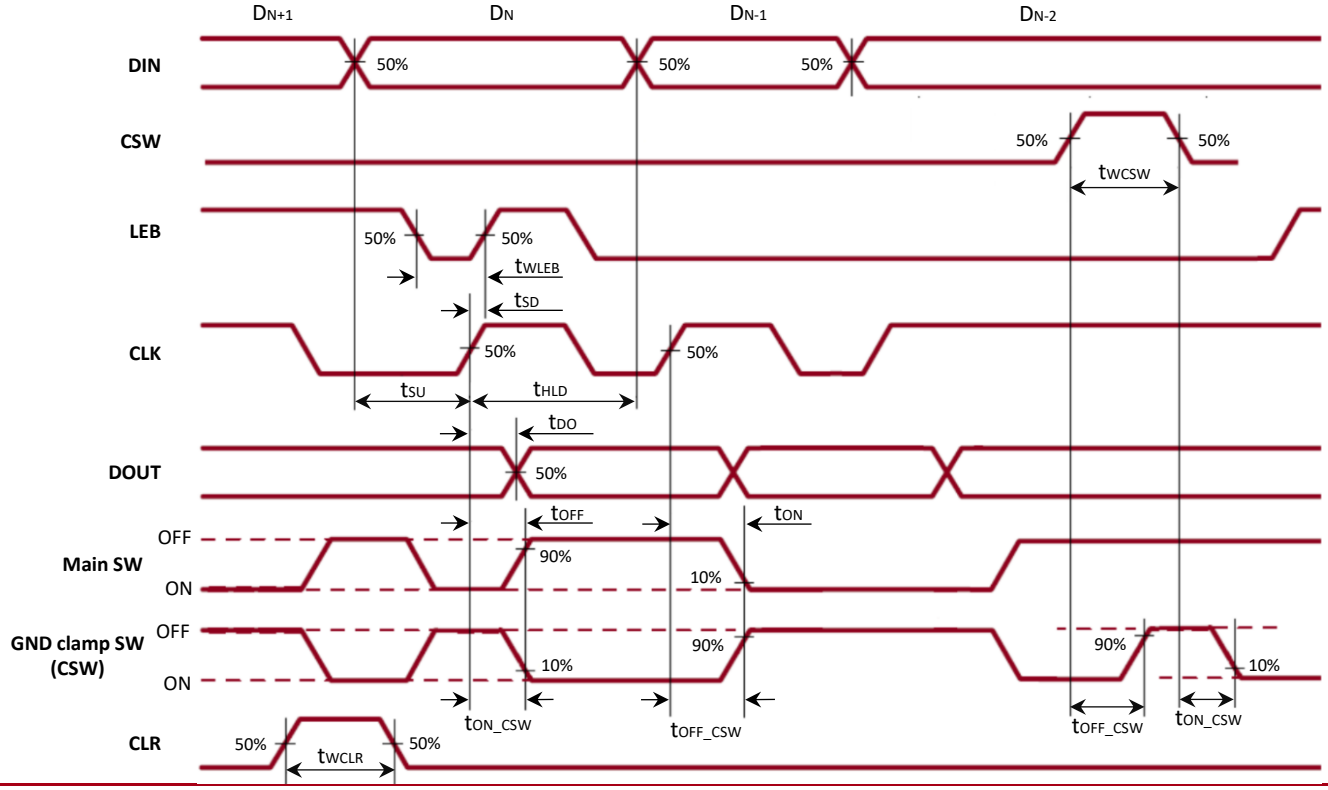


Output Voltage Spike Y

7, Logic Function Table

Logic Inputs										Analog Switch State											
LEB	CLR	CSW	DIN							SW0		SW1		...	SW32		SW33		...	SW63	
			D0	D1	...	D32	D33	...	D63	Main SW	Clamp SW	Main SW	Clamp SW	...	Main SW	Clamp SW	Main SW	Clamp SW	...	Main SW	Clamp SW
L	L	L	L	-		-	-		-	OFF	ON	-	-		-	-	-	-		-	-
L	L	L	H	-		-	-		-	ON	OFF	-	-		-	-	-	-		-	-
L	L	L	-	L		-	-		-	-	-	OFF	ON		-	-	-	-		-	-
L	L	L	-	H		-	-		-	-	-	ON	OFF		-	-	-	-		-	-
L	L	L	-	-		-	-		-	-	-	-	-		-	-	-	-		-	-
L	L	L	-	-		-	-		-	-	-	-	-		-	-	-	-		-	-
L	L	L	-	-		L	-		-	-	-	-	-		OFF	ON	-	-		-	-
L	L	L	-	-	...	H	-	...	-	-	-	-	-	...	ON	OFF	-	-	...	-	-
L	L	L	-	-		-	L		-	-	-	-	-		-	-	OFF	ON		-	-
L	L	L	-	-		-	H		-	-	-	-	-		-	-	ON	OFF		-	-
L	L	L	-	-		-	-		-	-	-	-	-		-	-	-	-		-	-
L	L	L	-	-		-	-		-	-	-	-	-		-	-	-	-		-	-
L	L	L	-	-		-	-		L	-	-	-	-		-	-	-	-		OFF	ON
L	L	L	-	-		-	-		H	-	-	-	-		-	-	-	-		ON	OFF
L	L	H	L	-		-	-		-	OFF	**OFF**	-	-		-	-	-	-		-	-
L	L	H	H	-		-	-		-	ON	OFF	-	-		-	-	-	-		-	-
L	L	H	-	L		-	-		-	-	-	OFF	**OFF**		-	-	-	-		-	-
L	L	H	-	H		-	-		-	-	-	ON	OFF		-	-	-	-		-	-
L	L	H	-	-		-	-		-	-	-	-	-		-	-	-	-		-	-
L	L	H	-	-		-	-		-	-	-	-	-		-	-	-	-		-	-
L	L	H	-	-		L	-		-	-	-	-	-		OFF	**OFF**	-	-		-	-
L	L	H	-	-	...	H	-	...	-	-	-	-	-	...	ON	OFF	-	-	...	-	-
L	L	H	-	-		-	L		-	-	-	-	-		-	-	OFF	**OFF**		-	-
L	L	H	-	-		-	H		-	-	-	-	-		-	-	ON	OFF		-	-
L	L	H	-	-		-	-		-	-	-	-	-		-	-	-	-		-	-
L	L	H	-	-		-	-		-	-	-	-	-		-	-	-	-		-	-
L	L	H	-	-		-	-		L	-	-	-	-		-	-	-	-		OFF	**OFF**
L	L	H	-	-		-	-		H	-	-	-	-		-	-	-	-		ON	OFF
H	L	X	X	X	X	X	X	X	X	Hold Previous State											
X	H	X	X	X	X	X	X	X	X	ALL "Main SWs" OFF											

8, Logic Timing Waveforms



9, Pin Configuration (MAP) 110-lead LGA

110-lead LGA
(Top view)

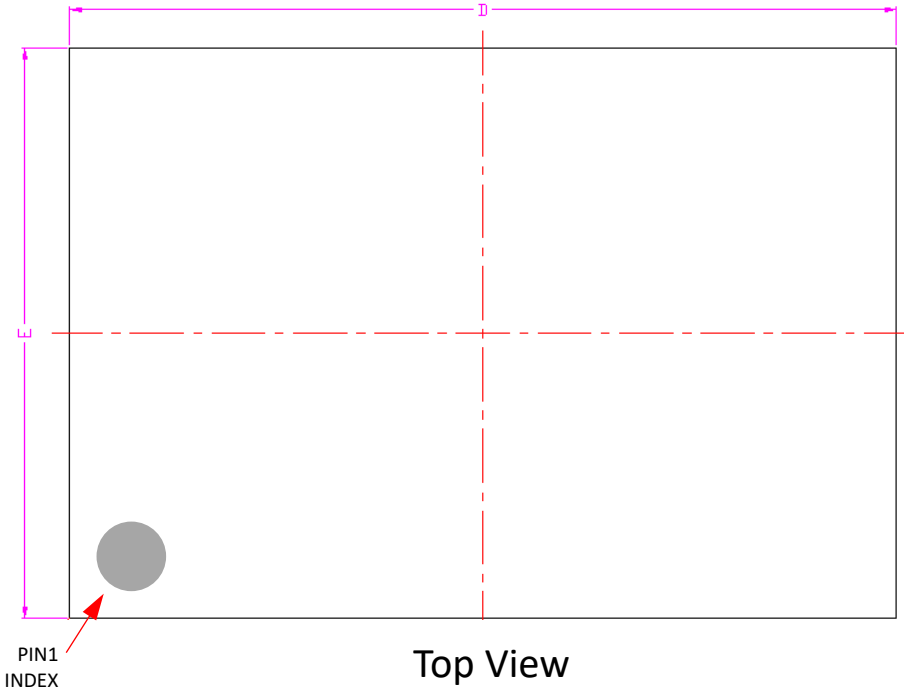
10, Pin Configuration (Table) 110-lead LGA

Pin#	Pin Name	I/O	Function
1	Y01	I/O	Analog switch terminal 0-1 (AFE side)
2	Y23	I/O	Analog switch terminal 2-3 (AFE side)
3	Y45	I/O	Analog switch terminal 4-5 (AFE side)
4	Y67	I/O	Analog switch terminal 6-7 (AFE side)
5	Y89	I/O	Analog switch terminal 8-9 (AFE side)
6	Y1011	I/O	Analog switch terminal 10-11 (AFE side)
7	Y1213	I/O	Analog switch terminal 12-13 (AFE side)
8	Y1415	I/O	Analog switch terminal 14-15 (AFE side)
9	Y1617	I/O	Analog switch terminal 16-17 (AFE side)
10	Y1819	I/O	Analog switch terminal 18-19 (AFE side)
11	Y2021	I/O	Analog switch terminal 20-21 (AFE side)
12	Y2223	I/O	Analog switch terminal 22-23 (AFE side)
13	Y2425	I/O	Analog switch terminal 24-25 (AFE side)
14	Y2627	I/O	Analog switch terminal 26-27 (AFE side)
15	Y2829	I/O	Analog switch terminal 28-29 (AFE side)
16	Y3031	I/O	Analog switch terminal 30-31 (AFE side)
17	Y3233	I/O	Analog switch terminal 32-33 (AFE side)
18	Y3435	I/O	Analog switch terminal 34-35 (AFE side)
19	Y3637	I/O	Analog switch terminal 36-37 (AFE side)
20	Y3839	I/O	Analog switch terminal 38-39 (AFE side)
21	Y4041	I/O	Analog switch terminal 40-41 (AFE side)
22	Y4243	I/O	Analog switch terminal 42-43 (AFE side)
23	Y4445	I/O	Analog switch terminal 44-45 (AFE side)
24	Y4647	I/O	Analog switch terminal 46-47 (AFE side)
25	Y4849	I/O	Analog switch terminal 48-49 (AFE side)
26	Y5051	I/O	Analog switch terminal 50-51 (AFE side)
27	Y5253	I/O	Analog switch terminal 52-53 (AFE side)
28	Y5455	I/O	Analog switch terminal 54-55 (AFE side)
29	Y5657	I/O	Analog switch terminal 56-57 (AFE side)
30	Y5859	I/O	Analog switch terminal 58-59 (AFE side)
31	Y6061	I/O	Analog switch terminal 60-61 (AFE side)
32	Y6263	I/O	Analog switch terminal 62-63 (AFE side)
33	GND	-	Drive power ground (0V)
34	VDD	-	Positive low voltage power supply (+5V)
35	VLL	-	Positive voltage supply of low voltage interface (+1.8V~+5V)
36	DOUT	O	Serial-Data output
37	CLR	I	Clear input
38	CSW	I	GND clamp control, Hi=always disabled, Low=main switches and GND clamp switches are alternately turned on and off
39	SW63	I/O	Analog switch terminal 63 (Probe side)
40	SW61	I/O	Analog switch terminal 61 (Probe side)
41	SW59	I/O	Analog switch terminal 59 (Probe side)
42	SW57	I/O	Analog switch terminal 57 (Probe side)
43	SW55	I/O	Analog switch terminal 55 (Probe side)
44	SW53	I/O	Analog switch terminal 53 (Probe side)
45	SW51	I/O	Analog switch terminal 51 (Probe side)
46	SW49	I/O	Analog switch terminal 49 (Probe side)
47	SW47	I/O	Analog switch terminal 47 (Probe side)
48	SW45	I/O	Analog switch terminal 45 (Probe side)
49	SW43	I/O	Analog switch terminal 43 (Probe side)
50	SW41	I/O	Analog switch terminal 41 (Probe side)
51	SW39	I/O	Analog switch terminal 39 (Probe side)
52	SW37	I/O	Analog switch terminal 37 (Probe side)
53	SW35	I/O	Analog switch terminal 35 (Probe side)
54	RGND	-	Bleed resistor ground (0V)
55	GND	-	Drive power ground (0V)

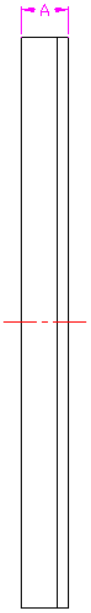
Pin#	Pin Name	I/O	Function
56	SW33	I/O	Analog switch terminal 33 (Probe side)
57	SW31	I/O	Analog switch terminal 31 (Probe side)
58	SW29	I/O	Analog switch terminal 29 (Probe side)
59	SW27	I/O	Analog switch terminal 27 (Probe side)
60	SW25	I/O	Analog switch terminal 25 (Probe side)
61	SW23	I/O	Analog switch terminal 23 (Probe side)
62	SW21	I/O	Analog switch terminal 21 (Probe side)
63	SW19	I/O	Analog switch terminal 19 (Probe side)
64	SW17	I/O	Analog switch terminal 17 (Probe side)
65	SW15	I/O	Analog switch terminal 15 (Probe side)
66	SW13	I/O	Analog switch terminal 13 (Probe side)
67	SW11	I/O	Analog switch terminal 11 (Probe side)
68	SW9	I/O	Analog switch terminal 9 (Probe side)
69	SW7	I/O	Analog switch terminal 7 (Probe side)
70	SW5	I/O	Analog switch terminal 5 (Probe side)
71	SW3	I/O	Analog switch terminal 3 (Probe side)
72	SW1	I/O	Analog switch terminal 1 (Probe side)
73	SW62	I/O	Analog switch terminal 62 (Probe side)
74	SW60	I/O	Analog switch terminal 60 (Probe side)
75	SW58	I/O	Analog switch terminal 58 (Probe side)
76	SW56	I/O	Analog switch terminal 56 (Probe side)
77	SW54	I/O	Analog switch terminal 54 (Probe side)
78	SW52	I/O	Analog switch terminal 52 (Probe side)
79	SW50	I/O	Analog switch terminal 50 (Probe side)
80	SW48	I/O	Analog switch terminal 48 (Probe side)
81	SW46	I/O	Analog switch terminal 46 (Probe side)
82	SW44	I/O	Analog switch terminal 44 (Probe side)
83	SW42	I/O	Analog switch terminal 42 (Probe side)
84	SW40	I/O	Analog switch terminal 40 (Probe side)
85	SW38	I/O	Analog switch terminal 38 (Probe side)
86	SW36	I/O	Analog switch terminal 36 (Probe side)
87	SW34	I/O	Analog switch terminal 34 (Probe side)
88	GND	-	Drive power ground (0V)
89	SW32	I/O	Analog switch terminal 32 (Probe side)
90	SW30	I/O	Analog switch terminal 30 (Probe side)
91	SW28	I/O	Analog switch terminal 28 (Probe side)
92	SW26	I/O	Analog switch terminal 26 (Probe side)
93	SW24	I/O	Analog switch terminal 24 (Probe side)
94	SW22	I/O	Analog switch terminal 22 (Probe side)
95	SW20	I/O	Analog switch terminal 20 (Probe side)
96	SW18	I/O	Analog switch terminal 18 (Probe side)
97	SW16	I/O	Analog switch terminal 16 (Probe side)
98	SW14	I/O	Analog switch terminal 14 (Probe side)
99	SW12	I/O	Analog switch terminal 12 (Probe side)
100	SW10	I/O	Analog switch terminal 10 (Probe side)
101	SW8	I/O	Analog switch terminal 8 (Probe side)
102	SW6	I/O	Analog switch terminal 6 (Probe side)
103	SW4	I/O	Analog switch terminal 4 (Probe side)
104	SW2	I/O	Analog switch terminal 2 (Probe side)
105	SW0	I/O	Analog switch terminal 0 (Probe side)
106	GND	-	Drive power ground (0V)
107	DIN	I	Serial-Datain put
108	LEB	I	Active Low latch enable input, Hi=Hold data, Low=Latch data input
109	CLK	I	Serial-Clock input
110	GND	-	Drive power ground (0V)

11, 110-Lead LGA Package Outline

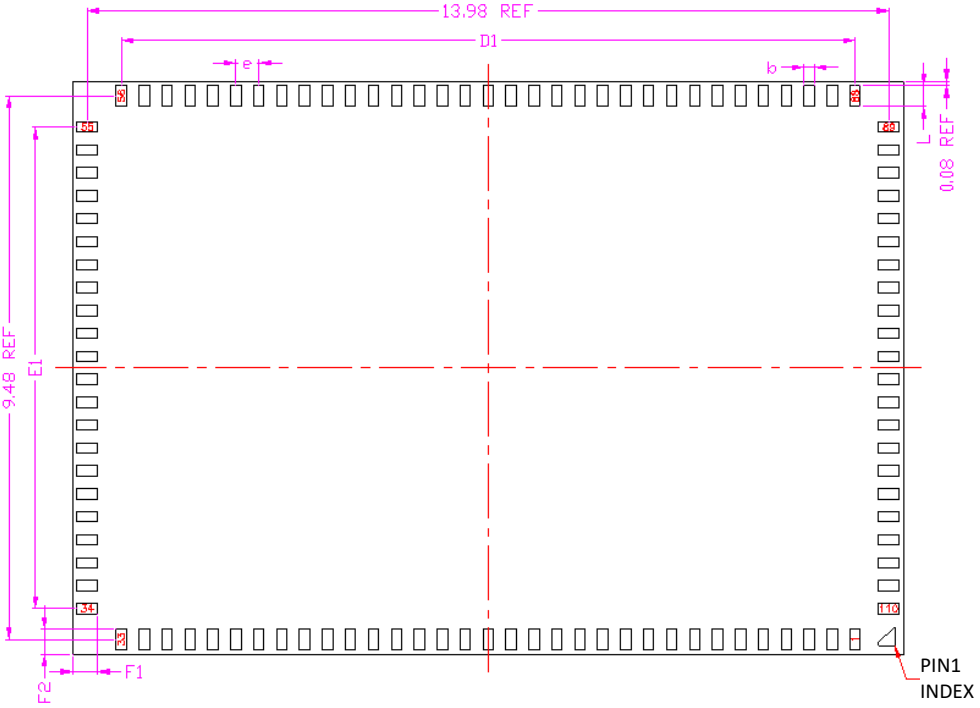
14.50 x 10.00mm body, 0.90mm height (max), 0.40mm pitch



Top View



Side View



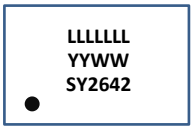
Bottom View

Note:

1) All dimensions are in millimeters.
2) Lead coplanarity shall be 0.10 millimeters Max.
3) JEDEC reference is MO-275A.
4) Deawing is not to scale.

Symbol		D	E	A	D1	E1	e	L	b	F1	F2
Dimension (mm)	Min	14.40	9.90	---	12.70	8.30	0.40 BSC.	0.30	0.12	0.37	0.37
	Nom	14.50	10.00	0.80	12.80	8.40		0.36	0.18	0.44	0.44
	Max	14.60	10.10	0.90	12.90	8.50		0.42	0.24	0.51	0.51

12, Product Marking



L = Lot Number
YY = Year Sealed
WW = Week Sealed

110-Lead LGA

13, Product Identification Information

PART NO.	XX	XX
Device	Package	Media Type

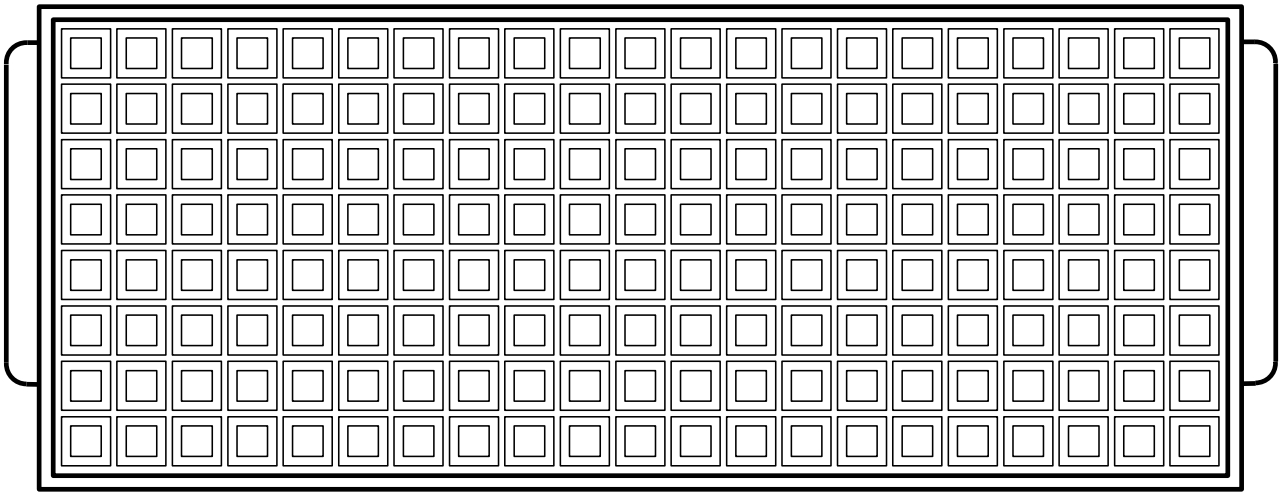
Device: SY2642: 64-Channel SPDT High Voltage Analog Switch

Package: GA: LGA

Media Type: (blank): 1680pcs for MOQ

Examples:

SY2642GA: 64-Channel SPDT High Voltage Analog Switch
110-lead LGA, 14.5x10.0mm
168pcs/Tray x10 for MOQ



Revision History

Revision #	Revision Date	Pages Updated	Description
Rev. 0.0	2026-01-26		Initially released