8通道，3电平，集成有源T/R开关的脉冲发生器

特性：

- 0至±100V输出电压
- ±2A输出峰值电流（VPP/VNN）
- ±1A的有源接地箝位峰值电流
- 250Ω(±0.1A)有源接地钳位
- 嵌入式浮地稳压器
- 低二次谐波失真的对称正负脉冲波形
- 支持高达200MHz LVDS/LVCMOS 时钟（支持透明模式）
- 15Ω有源T/R开关，具备2位开启时序控制
- 在±60V输出，220pF负载下支持20MHz输出频率
- 1.8V至5V CMOS逻辑接口
- 每个高压输出端均有降噪二极管
- 输出电流具有4种控制模式
- 集成指示功能的自动过热保护
- 上电/断电复位功能，用于自由上电排序和突然断电时的故障保护
- 采用SOI CMOS技术，通道间无闩锁、低串扰
- 64引脚 9x9mm QFN封装

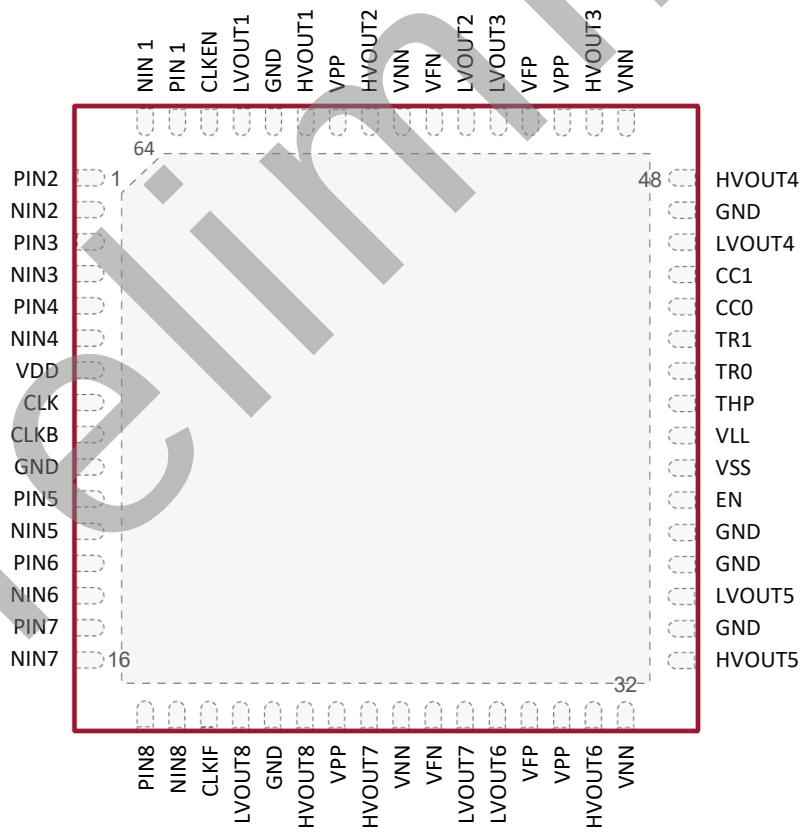
概述：

SY5817是一款八进制，3电平，高压，高速，集成T/R开关的8通道单片高压高速脉冲发生器，内置快速回零阻尼场效应管，该高压高速芯片不仅适用于便携式医学超声成像设备，也适用于无损检测和测试设备应用。
每个通道的输出峰值电流都达到±2A以上，脉冲电压可达±100V，并具有归零模式。
SY5817包括逻辑接口，电平转换器，带浮动稳压器的MOSFET栅极驱动器，高压大电流的MOSFET和有源T/R开关。

应用：

- 医疗超声影像
- 无损探伤
- 压电传感器驱动
- 光学MEMS模组

Pin Configuration



64-lead QFN
(Top view)

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Pin Configuration

Table 1 Pin Configuration

Pin#	Pin Name	I/O	Function
1	PIN2	I	Logic input of channel 2
2	NIN2	I	Logic input of channel 2
3	PIN3	I	Logic input of channel 3
4	NIN3	I	Logic input of channel 3
5	PIN4	I	Logic input of channel 4
6	NIN4	I	Logic input of channel 4
7	VDD	-	Positive low voltage power supply (+5V)
8	CLK	I	Positive clock input (up to 200MHz)
9	CLKB	I	Negative clock Input (up to 200MHz)
10	GND	-	Drive power ground (0V)
11	PIN5	I	Logic input of channel 5
12	NIN5	I	Logic input of channel 5
13	PIN6	I	Logic input of channel 6
14	NIN6	I	Logic input of channel 6
15	PIN7	I	Logic input of channel 7
16	NIN7	I	Logic input of channel 7
17	PIN8	I	Logic input of channel 8
18	NIN8	I	Logic input of channel 8
19	CLKIF	I	Control of clock interface, Hi=differential CMOS, Low=LVDS (50kΩ internal pull-up resistor)
20	LVOUT8	O	Low voltage output of channel 8
21	GND	-	Drive power ground (0V)
22	HVOUT8	I/O	High voltage output of channel 8
23	VPP	-	Positive high voltage power supply (0 to +100V)
24	HVOUT7	I/O	High voltage output of channel 7
25	VNN	-	Negative high voltage power supply (0 to -100V)
26	VFN	-	Built-in power supply for N-MOS (N1) gate drive
27	LVOUT7	O	Low voltage output of channel 7
28	LVOUT6	O	Low voltage output of channel 6
29	VFP	-	Built-in power supply for P-MOS (P1) gate drive
30	VPP	-	Positive high voltage power supply (0 to +100V)
31	HVOUT6	I/O	High voltage output of channel 6
32	VNN	-	Negative high voltage power supply (0 to -100V)

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Pin Configura tion (Continued)

Pin#	Pin Name	I/O	Function
33	HVOUT5	I/O	High voltage output of channel 5
34	GND	-	Drive power ground (0V)
35	LVOUT5	O	Low voltage output of channel 5
36	GND	-	Drive power ground (0V)
37	GND	-	Drive power ground (0V)
38	EN	I	Control of drive output enable, Hi=off, Low=on (50kΩ internal pull-up resistor)
39	VSS	-	Negative low voltage power supply (-5V)
40	VLL	-	Positive voltage supply of logic input interface (1.8 to 5V)
41	THP	O	Thermal protection output flag, open N-MOS drain
42	TR0	I	Lower bit of control of T/R switch S1 and S2 turn-on overlap time (50kΩ internal pull-down resistor)
43	TR1	I	Upper bit of control of T/R switch S1 and S2 turn-on overlap time (50kΩ internal pull-down resistor)
44	CC0	I	Lower bit of control of P1/N1 drive current (50kΩ internal pull-up resistor)
45	CC1	I	Upper bit of control of P1/N1 drive current (50kΩ internal pull-up resistor)
46	LVOUT4	O	Low voltage output of channel 4
47	GND	-	Drive power ground (0V)
48	HVOUT4	I/O	High voltage output of channel 4
49	VNN	-	Negative high voltage power supply (0 to -100V)
50	HVOUT3	I/O	High voltage output of channel 3
51	VPP	-	Positive high voltage power supply (0 to +100V)
52	VFP	-	Built-in power supply for P-MOS (P1) gate drive
53	LVOUT3	O	Low voltage output of channel 3
54	LVOUT2	O	Low voltage output of channel 2
55	VFN	-	Built-in power supply for N-MOS (N1) gate drive
56	VNN	-	Negative high voltage power supply (0 to -100V)
57	HVOUT2	I/O	High voltage output of channel 2
58	VPP	-	Positive high voltage power supply (0 to +100V)
59	HVOUT 1	I/O	High voltage output of channel 1
60	GND	-	Drive power ground (0V)
61	LVOUT 1	O	Low voltage output of channel 1
62	CLKEN	I	Control of clock enable, Hi=clock disable, Low=clock enable (50kΩ internal pull-up resistor)
63	PIN 1	I	Logic input of channel 1
64	NIN 1	I	Logic input of channel 1

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◆ 功能方框图：

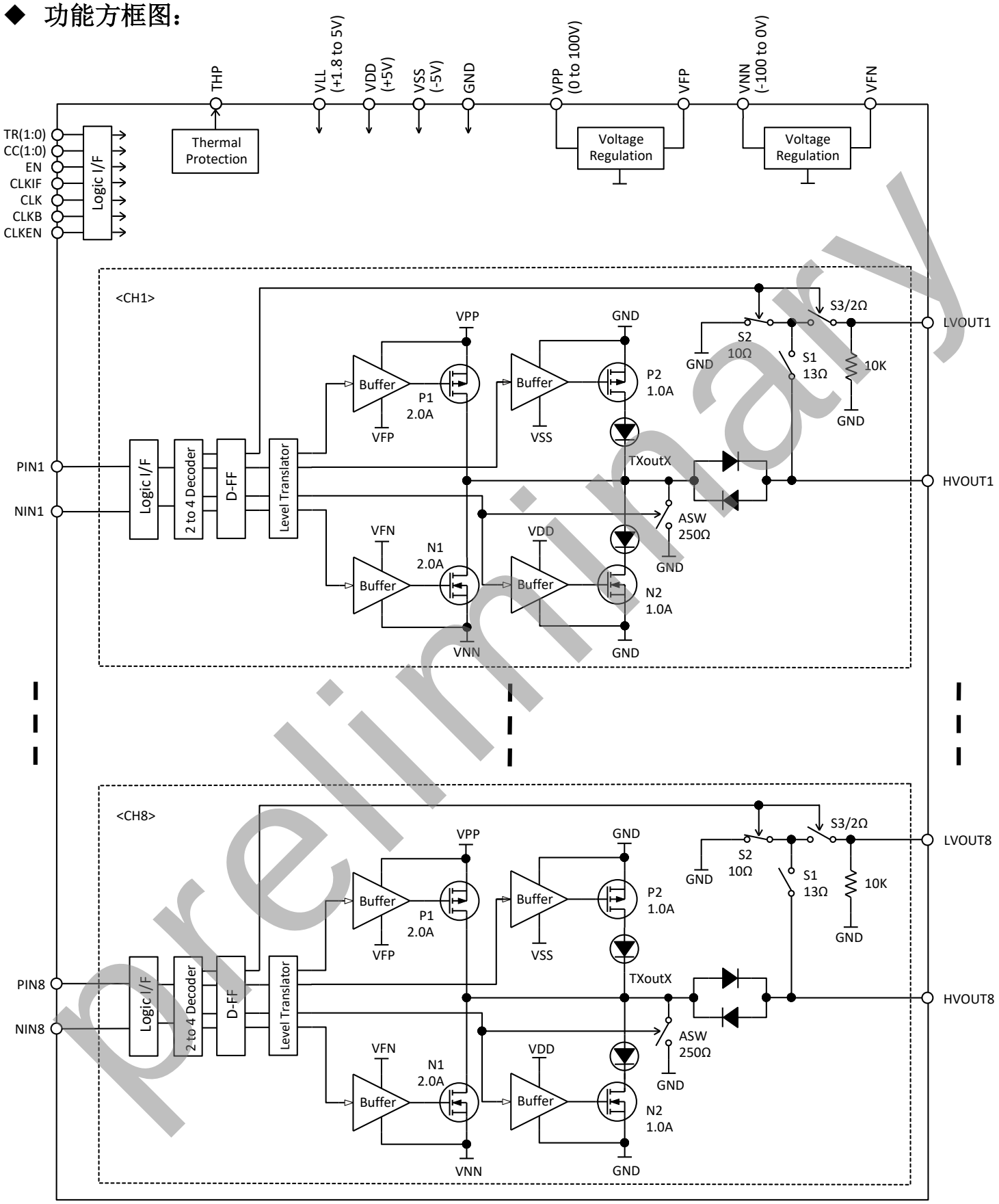

Fig.1 方框图

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1，极限范围

T_A=25℃, unless otherwise specified

Absolute Maximum Ratings

Substrate (VSUB, connect to GND) 0V
All Logic I/O and CLK Pins (PINx, NINx, EN, CLKEN, CLK,CLKB, CLKIF, CC(1:0), TR(1:0)) ..... -0.4V to +7.0V
V_{LL} Logic Supply Voltage ..... -0.4V to +7.0V
V_{DD} Positive Supply Voltage ..... -0.4V to +7.0V
V_{SS} Negative Supply Voltage ..... -7.0V to +0.4V
V_{PP} Positive high-voltage supplies ..... -0.5V to +105V
V_{NN} Negative high-voltage supplies ..... -105V to +0.5V
$HVOUT_X$ High-voltage outputs (x=1~8) ..... -105V to +105V
$LVOUT_X$ Low-voltage outputs (x=1~8) ..... -1V to +1V
THP (Thermal Protection) output ..... -0.4V to +7.0V
T_{JOP} Operating junction temperature Range ..... -20 ℃ to +105 ℃
TA Operating free-air Temperature Range ..... 0 ℃ to +75 ℃
T_{STG} Storage Temperature Range ..... -55℃ to +150 ℃
P_{Dmax} Maximum power dissipation 5W

注意： 超出极限范围的应力可能会对产品造成永久性损坏。

2, Electrical Characteristics

Electrical Specifications:V_{LL}=2.5V, V_{DD}/V_{SS}=+/-5V, V_{PP}/V_{NN}=+/-60V, T_A=25°C, unless otherwise specified.

Items	Symbol	Spec			Units	Conditions
		Min	Typ	Max		
Operating Supply Voltages						
Logic supply voltage	V_{LL}	2.4	2.5 to 3.3	3.6	V	Clock mode
		1.7	1.8 to 5	V_{DD}	V	Transparent mode
Positive supply voltage	V_{DD}	4.75	5	5.25	V	
Negative supply voltage	V_{SS}	-5.25	-5	-4.75	V	
Positive high-voltage supplies	V_{PP}	0	-	100	V	
Negative high-voltage supplies	V_{NN}	-100	-	0	V	
IC substrate voltage	V_{SUB}	-	0	-	V	Thermal pad on the bottom of the package must be soldered to the ground.
V_{PP} , V_{NN} slew rate	SR_{MAX}	-	-	25	V/ms	

NOTE: Thermal pad on the bottom of the package must be soldered to the ground.

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Electrical Characteristics (Continued)

Electrical Specifications: V_{LL}=2.5V, V_{DD}/V_{SS}=+/-5V, V_{PP}/V_{NN}=+/-60V, T_A=25°C, unless otherwise specified.

Items		Symbol	Spec			Units	Conditions
			Min	Typ	Max		
Operating Supply Currents							
V_{LL} current	TP	I_{LLQD}	-	0.03	-	mA	Quiescent current-1
	LVDS CLK		-	0.08	-	mA	
	CMOS CLK		-	0.13	-	mA	
V_{DD} current	TP	I_{DDQD}	-	2.8	-	mA	EN=1(Disable) PINx=NINx=0 Current mode 3 (CC[1:0]='11') V_{PP}/V_{NN}=+/-100V
	LVDS CLK		-	2.8	-	mA	
	CMOS CLK		-	2.8	-	mA	
V_{SS} current		I_{SSQD}	-	0.63	-	mA	
V_{PP} current		I_{PPQD}	-	0.03	-	mA	
V_{NN} current		I_{NNQD}	-	0.04	-	mA	
V_{LL} current	TP	I_{LLQE}	-	0.08	-	mA	Quiescent current-2
	LVDS CLK		-	0.18	-	mA	
	CMOS CLK		-	0.13	-	mA	
V_{DD} current	TP	I_{DDQE}	-	10	-	mA	EN=0(Enable) PINx=NINx=0 Current mode 3 (CC[1:0]='11') V_{PP}/V_{NN}=+/-100V
	LVDS CLK		-	30	-	mA	
	CMOS CLK		-	28	-	mA	
V_{SS} current		I_{SSQE}	-	9.3	-	mA	
V_{PP} current		I_{PPQE}	-	0.15	-	mA	
V_{NN} current		I_{NNQE}	-	0.15	-	mA	
V_{LL} current	TP	I_{LLPW}	-	0.08	-	mA	PW operating current
	LVDS CLK		-	0.18	-	mA	
	CMOS CLK		-	0.13	-	mA	
V_{DD} current	TP	I_{DDPW}	-	10	-	mA	EN=0 Current mode 3 (CC[1:0]='11') 8-channel active Bipolar 3-level 2-cycle f=5MHz, PRT=200µs V_{PP}/V_{NN}=+/-60V
	LVDS CLK		-	34	-	mA	
	CMOS CLK		-	32	-	mA	
V_{SS} current		I_{SSPW}	-	9.3	-	mA	
V_{PP} current		I_{PPPW}	-	4.2	-	mA	
V_{NN} current		I_{NNPW}	-	4.9	-	mA	
V_{LL} current	TP	I_{LLCW3}	-	0.43	-	mA	CW operating current-1
	LVDS CLK		-	0.53	-	mA	
	CMOS CLK		-	0.48	-	mA	
V_{DD} current	TP	I_{DDCW3}	-	42	-	mA	EN=0 Current mode 3 (CC[1:0]='11') 8-channel active Bipolar 3-level Continuous f=5MHz V_{PP}/V_{NN}=+/-5V
	LVDS CLK		-	64	-	mA	
	CMOS CLK		-	61	-	mA	
V_{SS} current		I_{SSCW3}	-	27	-	mA	
V_{PP} current		I_{PPCW3}	-	217	-	mA	
V_{NN} current		I_{NNCW3}	-	220	-	mA	
V_{LL} current	TP	I_{LLCW2}	-	0.48	-	mA	CW operating current-2
	LVDS CLK		-	0.58	-	mA	
	CMOS CLK		-	0.53	-	mA	
V_{DD} current	TP	I_{DDCW2}	-	38	-	mA	EN=0 Current mode 2 (CC[1:0]='10') 8-channel active Bipolar 3-level Continuous f=5MHz V_{PP}/V_{NN}=+/-5V
	LVDS CLK		-	60	-	mA	
	CMOS CLK		-	57	-	mA	
V_{SS} current		I_{SSCW2}	-	23	-	mA	
V_{PP} current		I_{PPCW2}	-	208	-	mA	
V_{NN} current		I_{NNCW2}	-	211	-	mA	

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Electrical Characteristics (Continued)

Electrical Specifications: V_{LL}=2.5V, V_{DD}/V_{SS}=+/-5V, V_{PP}/V_{NN}=+/-60V, T_A=25°C, unless otherwise specified.

Items		Symbol	Spec			Units	Conditions
			Min	Typ	Max		
V_{LL} current	TP	I_{LLCW1}	-	0.48	-	mA	CW operating current-3 EN=0 Current mode 1 (CC[1:0]='01') 8-channel active Bipolar 3-level Continuous f=5MHz V_{PP}/V_{NN}=+/-5V
	LVDS CLK		-	0.58	-	mA	
	CMOS CLK		-	0.53	-	mA	
V_{DD} current	TP	I_{DDCW1}	-	34	-	mA	
	LVDS CLK		-	56	-	mA	
	CMOS CLK		-	53	-	mA	
V_{SS} current		I_{SSCW1}	-	18	-	mA	
V_{PP} current		I_{PPCW1}	-	195	-	mA	
V_{NN} current		I_{NNCW1}	-	198	-	mA	
V_{LL} current	TP	I_{LLCW0}	-	0.53	-	mA	CW operating current-4 EN=0 Current mode 0 (CC[1:0]='00') 8-channel active Bipolar 3-level Continuous f=5MHz V_{PP}/V_{NN}=+/-5V
	LVDS CLK		-	0.63	-	mA	
	CMOS CLK		-	0.58	-	mA	
V_{DD} current	TP	I_{DDCW0}	-	28	-	mA	
	LVDS CLK		-	49	-	mA	
	CMOS CLK		-	47	-	mA	
V_{SS} current		I_{SSCW0}	-	13	-	mA	
V_{PP} current		I_{PPCW0}	-	169	-	mA	
V_{NN} current		I_{NNCW0}	-	173	-	mA	
T/R Switch							
$LVOUT_X$ output voltage range		$LVOUT_X$	-0.85	-	.+0.85	V	
TRSW on-resistance		R_{OUTR}	-	15	-	Ω	$HVOUT_X$=100mV, $LVOUT_X$=0V
TRSW on-capacitance		C_{OUTR}	-	12	-	pF	$LVOUT_X$=0V
TRSW off-resistance on $HVOUT_X$		$R_{OFFTRHV}$	1	-	-	MΩ	
TRSW off-resistance on $LVOUT_X$		$R_{OFFTRLV}$	8	10	12	kΩ	
Spike voltage on $LVOUT_X$ and $LVOUT_X$		V_{TRN}	-	-	50	mV_{PP}	50pF//200Ω load on $HVOUT_X$ 20pF//200Ω load on $LVOUT_X$
TRSW turn-on time	TR[1:0]='00'	t_{dTRON}	-	300	-	ns	Logic input-to-ready for Rx signal See Fig.6
	TR[1:0]='01'		-	400	-	ns	
	TR[1:0]='10'		-	500	-	ns	
	TR[1:0]='11'		-	600	-	ns	
TRSW turn-off time		t_{dTROFF}	-	50	100	ns	See Fig.6
Tx setup time		t_{TXSU}	100	-	-	ns	PIN_X=NIN_X=0 (GND) for at least 100ns before Tx burst. See Fig.6
Analog Switch							
ASW on-resistance		R_{ONASW}	-	250	-	Ω	
HV Blocking Diode							
Forward voltage		V_{FHVD}	-	1.0	-	V	I_F=100mA
			-	1.2	-	V	I_F=200mA
Reverse voltage		V_{RHVD}	200	-	-	V	I_R=1uA
LV Noise-cut Diode							
Forward voltage		V_{FLVD}	-	1.00	-	V	IF=100mA
			-	1.25	-	V	IF=200mA

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Electrical Characteristics (Continued)

Electrical Specifications: V_{LL}=2.5V, V_{DD}/V_{SS}=+/-5V, V_{PP}/V_{NN}=+/-60V, T_A=25°C, unless otherwise specified.

Items		Symbol	Spec			Units	Conditions	
			Min	Typ	Max			
Timing Characteristics								
Output frequency		f_{OUT}	-	20.0	-	MHz		
Output rise propagation delay	TP mode	t_{dr}	-	31.0	-	ns	See Fig.4	
	CLK mode		-	37.0	-	ns		
Output fall propagation delay	TP mode	t_{df}	-	31.0	-	ns		
	CLK mode		-	37.0	-	ns		
Output rise propagation delay clamp	TP mode	t_{drCL}	-	31.0	-	ns		
	CLK mode		-	37.0	-	ns		
Output fall propagation delay clamp	TP mode	t_{dfCL}	-	31.0	-	ns		
	CLK mode		-	37.0	-	ns		
Propagation delay matching		Δt_d	-	±1	±3	ns		
Output rise time		t_r	-	16	-	ns	CC[1:0]='11'	See Fig.4
			-	24	-	ns	CC[1:0]='10'	
			-	34	-	ns	CC[1:0]='01'	
			-	44	-	ns	CC[1:0]='00'	
		t_{rCL}	-	25	-	ns		
Output fall time		t_f	-	16	-	ns	CC[1:0]='11'	
			-	24	-	ns	CC[1:0]='10'	
			-	34	-	ns	CC[1:0]='01'	
			-	44	-	ns	CC[1:0]='00'	
		t_{fCL}	-	25	-	ns		
2nd harmonic distortion		HD2	-	-40	-	dBc	Bipolar, 2-cyc, f_{OUT}=5MHz	
Pulse cancellation		HDPC	-	-40	-	dBc		
		HDPC2	-	-40	-	dBc		
RMS output jitter		t_J	-	10	-	ps	Bipolar CW, f_{OUT}=5MHz V_{PP}/V_{NN}=+/-5V	
Crosstalk between channels		X_{TLK}	-	-70	-	dB	f_{OUT}=5MHz, 10Vp-p HV_{OUT} load =50Ω	
Output enable time	TP	t_{EN}	-	31	-	ns	See Fig.5	
	LVDS CLK		-	120	-	ns		
	CMOS CLK		-	140	-	ns		
Output disable time		t_{DS}	-	37	-	ns		
Clock mode enable time		t_{CLKEN}	-	37	-	ns		
Clock mode disable time		t_{CLKDS}	-	37	-	ns		

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3, Clock Mode / Transparent Mode

Clock (CLK) mode synchronizes data inputs PINX, NINX (X=1~8) with a differential LVDS/CMOS clock. Transparent (TP) mode without using clock is also available.

CLK mode:

Set CLKEN=0. PINX and NINX are decoded, clocked, level-translated, then sent to high-voltage output stage. Differential clock input has two modes as shown below.

- LVDS CLK mode: set CLKIF=0. Connect 100Ω between CLK and CLKB. See Table 3 and 4 for the logic inputs, CLK, and CLKB.
- CMOS CLK mode: set CLKIF=1. See Table 3 for all the logic inputs.

TP mode:

Set CLKEN=CLKIF=1, CLK=CLKB=0. PINX and NINX are decoded, level-translated, then sent to high-voltage output stage.
See Table 3 for all the logic inputs.

Table 3 Logic Inputs

No	Items	Symbol	Min	Typ	Max	Units	Condition	
1	High-level logic input voltage	V_{IH}	0.8V_{LL}	-	V_{LL}	V		
2	Low-level logic input voltage	V_{IL}	0	-	0.2V_{LL}	V		
3	Logic input capacitance	C_{IN}	-	3	-	pF		
4	Logic input high current *1	I_{IH}	-10	-	10	μA		
5	Logic input low current *2	I_{IL}	-10	-	10	μA		
6	Input rise/fall time	tr, tf	-	-	800	ps	CLK≥100MHz	CMOS CLK mode 10~90% CLK, CLKB, PINX, NINX
			-	-	2.0	ns	CLK<100MHz	
7	Input clock frequency	f_{CLK}	-	-	200	MHz	CMOS CLK mode, CLK, CLKB, f_{CLK}=1/T, D_{CLK}=τ/T, See Fig.4	
8	Duty cycle	D_{CLK}	40	50	60	%		
9	Data Setup time	t_{SU}	1.4	-	-	ns	CLK mode, PINX, NINX to CLK/CLKB See Fig.4	
10	Data Hold time	t_{HLD}	1.4	-	-	ns		

NOTE:
1) TR[1:0] have 50μA leakage at V_{LL}=2.5V due to 50kΩ internal pull-down resistor.
2) EN, CC[1:0], CLKEN, and CLKIF have 50μA leakage at V_{LL}=2.5V due to 50kΩ internal pull-up resistor.

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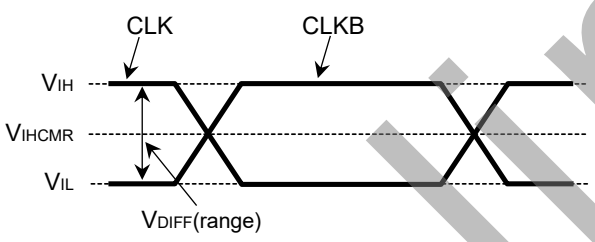
Table 4 LVDS Clock Inputs (CLK, CLKB)

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	High-level input voltage	V_{IH}	1.265	-	-	V	V_{IHCMR}(Typ)+V_{DIFF}(Min)/2
2	Low-level input voltage	V_{IL}	-	-	1.135	V	V_{IHCMR}(Typ)-V_{DIFF}(Min)/2
3	Differential input voltage range	$V_{DIFF(range)}$	0.13	0.35	0.49	±V	same as CLK, CLKB voltage swing See Fig.2
4	Differential input voltage peak to peak swing	$V_{DIFF(p-p)}$	0.26	0.7	0.98	Vpp	|CLK-CLKB| differential peak-to-peak voltage swing, See Fig.2
5	Input voltage common mode range	V_{IHCMR}	0.84	1.2	1.56	V	
6	Differential input impedance	R_{IN}	85	100	115	Ω	
7	High-level input current	I_{IH}	-	-	5.8	mA	
8	Low-level input current	I_{IL}	-	-	5.8	mA	
9	Input rise/fall time	t_r, t_f	-	-	600	ps	20% to 80% of V_{DIFF}
10	Input clock frequency	f_{CLK}	-	-	200	MHz	LVDS CLK mode, CLK, CLKB, f_{CLK}=1/T, D_{CLK}=τ /T, See Fig.4
11	Duty cycle	D_{CLK}	40	50	60	%	

NOTE: Please refer to table 3 for the logic inputs other than CLK, CLKB in LVDS CLK mode.

Differential input voltage range (V_{DIFF}(range)



Differential input voltage peak to peak swing (V_{DIFF}(p-p)

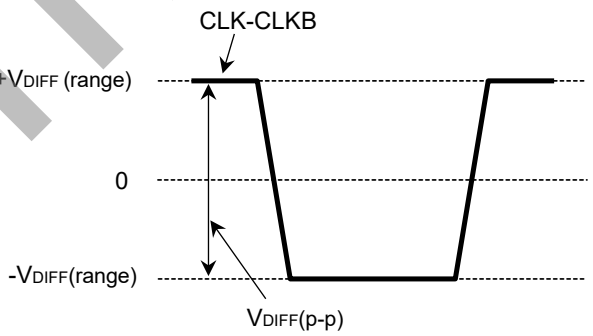


Fig.2 LVDS clock inputs

4, Power Supply Sequencing

Embedded low-voltage (LV) power-up/down reset function provides free power supply sequencing.

It also provides fail-safe system in abrupt LV power supply drop.
When any one of LV power supplies is turned off during operation, all internal circuits will be immediately reset, and both inputs and outputs will be disabled.

Once all LV power supplies are restored, both inputs and outputs will be enabled.

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5, Typical Application Circuit

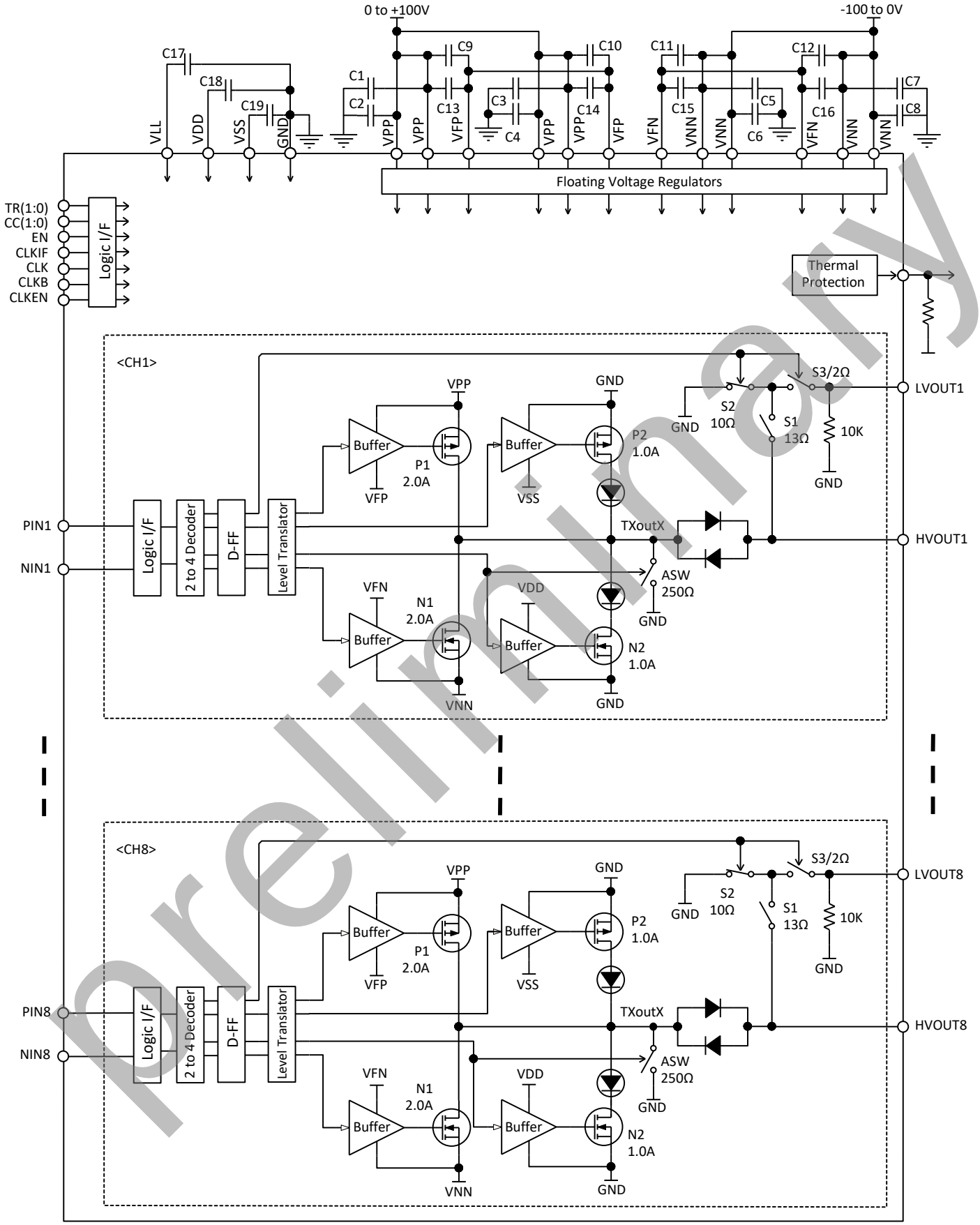

Fig.3 Typical Application Circuit

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Note:

1. High-voltage power supply pins, V_{PP}/V_{NN}, can draw fast transient currents up to ±2.0A. Therefore, ceramic capacitors of ≥200V 0.1µF to 1µF (C1~8) should be connected as close to the pins as possible for bypassing purpose.
2. Ceramic capacitors of ≥16V 10µF (C9~12), ≥16V 100nF (C13~16), and ≥16V 0.1µF to 1µF (C17~19) should also be connected between high-voltage power supply pins and corresponding floating voltage pins V_{FP}/V_{FN}, and lowvoltage power supply pins for bypassing purpose. Connect those as close to the pins as possible.
3. It is also important to minimize the trace length and to have enough trace width of those high voltage and floating voltage lines.
4. The thermal tab on the bottom of the package must be soldered to the GND.
5. Please refer to Mode Control Tables for detailed CC[1:0] and TR[1:0] setting.

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6, Static Characteristics

Table 6 Static Characteristics

V_{LL}=2.5V, V_{DD}/V_{SS}=+/-5V, T_A=25°C, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	HVOUTx output voltage range	HVOUTX	-100	-	.+100	V	
2	HVOUTx high-side peak current	IOH	-	2.0	-	A	VPP/VNN=+/-60V Current mode 3 (CC[1:0]='11')
			-	1.5	-	A	VPP/VNN=+/-60V Current mode 2 (CC[1:0]='10')
			-	1.0	-	A	VPP/VNN=+/-60V Current mode 1 (CC[1:0]='01')
			-	0.5	-	A	VPP/VNN=+/-60V Current mode 0 (CC[1:0]='00')
3	HVOUTx high-side GND clamp peak current	IOHCL	-	1.0	-	A	VPP/VNN=+/-60V
4	HVOUTx low-side peak current	IOL	-	2.0	-	A	VPP/VNN=+/-60V Current mode 3 (CC[1:0]='11')
			-	1.5	-	A	VPP/VNN=+/-60V Current mode 2 (CC[1:0]='10')
			-	1.0	-	A	VPP/VNN=+/-60V Current mode 1 (CC[1:0]='01')
			-	0.5	-	A	VPP/VNN=+/-60V Current mode 0 (CC[1:0]='00')
5	HVOUTx low-side GND clamp peak current	IOLCL	-	1.0	-	A	VPP/VNN=+/-60V
6	HVOUTx high-side on-resistance	RONH	-	10	-	Ω	IOH=100mA Current mode 3 (CC[1:0]='11')
			-	13	-	Ω	IOH=100mA Current mode 2 (CC[1:0]='11')
			-	18	-	Ω	IOH=100mA Current mode 1 (CC[1:0]='11')
			-	31	-	Ω	IOH=100mA Current mode 0 (CC[1:0]='11')
7	HVOUTx high-side GND clamp on-resistance	RONHCL	-	21	-	Ω	ICHCL=100mA
8	HVOUTx low-side on-resistance	RONL	-	9	-	Ω	IOL=100mA Current mode 3 (CC[1:0]='11')
			-	12	-	Ω	IOL=100mA Current mode 2 (CC[1:0]='11')
			-	17	-	Ω	IOL=100mA Current mode 1 (CC[1:0]='11')
			-	30	-	Ω	IOL=100mA Current mode 0 (CC[1:0]='11')
9	HVOUTx high-side GND clamp on-resistance	RONHCL	-	20	-	Ω	ICLCL=100mA
10	HVOUTx off-capacitance	CHVOFF	-	20	-	pF	TXOUTX=GND, TRSW=off

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7, Thermal Protection

Table 12 Thermal Protection Characteristics

V_{LL}=2.5V, V_{DD}/V_{SS}=+/-5V, T_A=25℃, unless otherwise specified.						
Items	**Symbol**	**Spec**			**Units**	**Conditions**
		Min	**Typ**	**Max**		
THP pull-up voltage	V_{PUTHP}	-	-	5.25	V	Open drain
THP output current	I_{THP}	-	1	-	mA	-
THP output low voltage	V_{OLTHP}	-	-	0.5	V	THP active, V_{LL}=2.5V, I_{THP}=1mA
THP temperature threshold	T_{THP}	90	110	130	℃	
THP reset hysteresis	T_{HYSTHP}	-	10	-	℃	

8, Setup/Hold Time and Switching Time Diagram

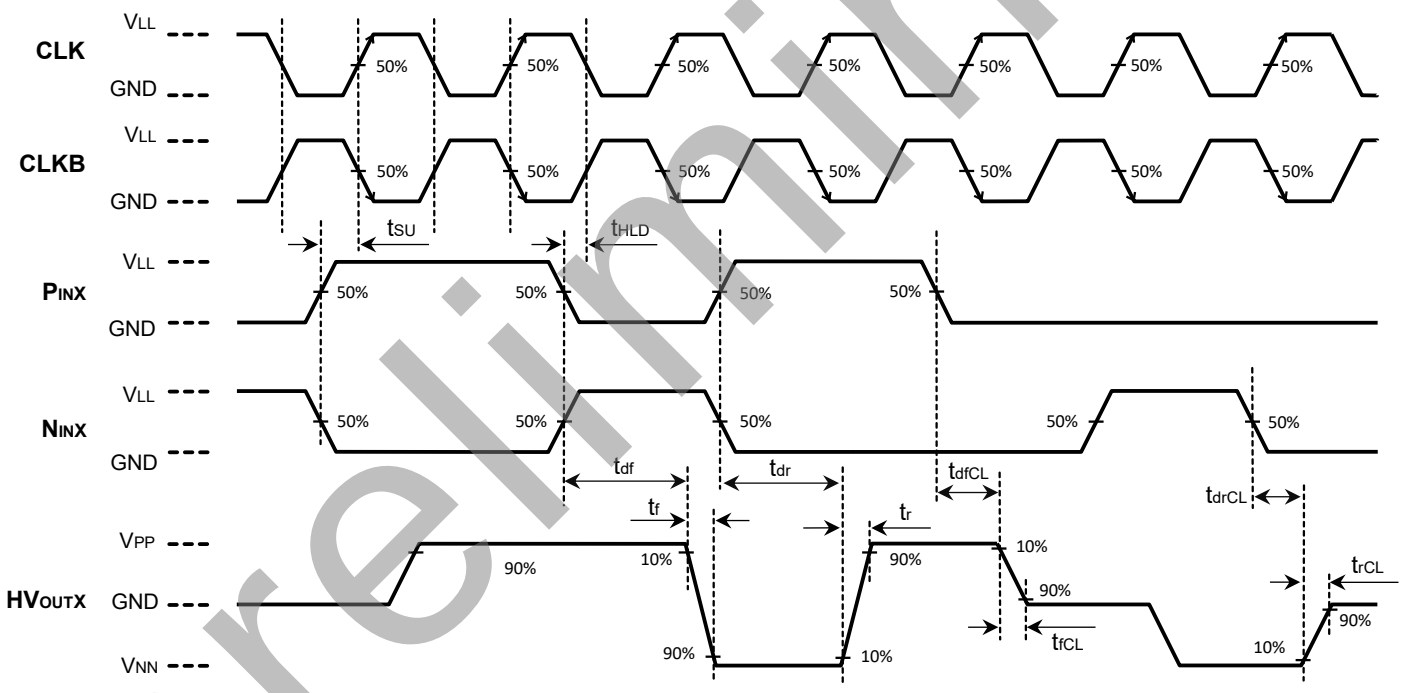

Fig.4 Setup/Hold Time and Propagation delay and Output rise/fall time

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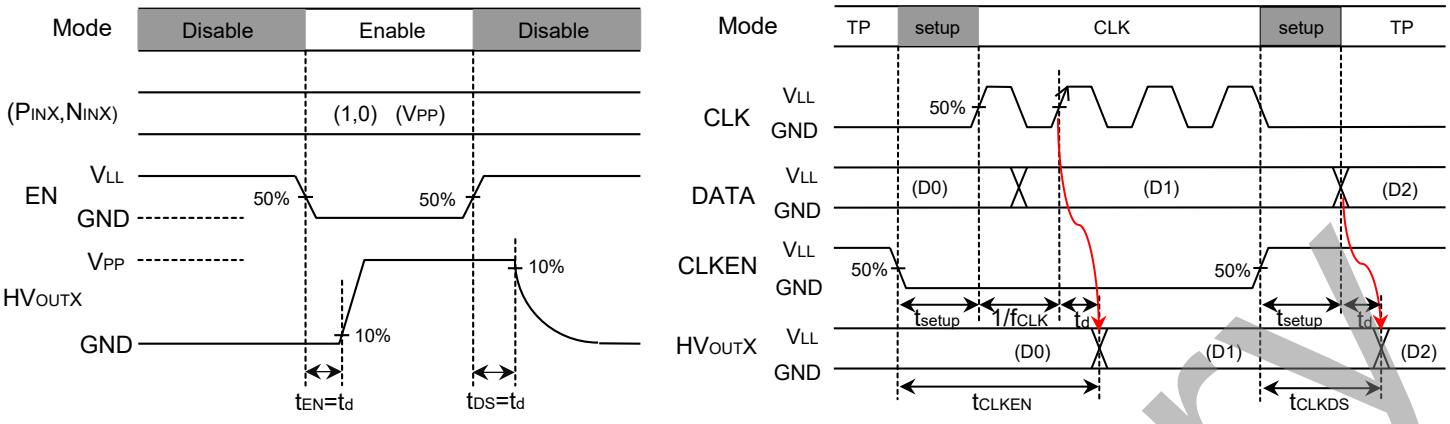

Fig.5 Output enable/disable and Clock enable/disable time

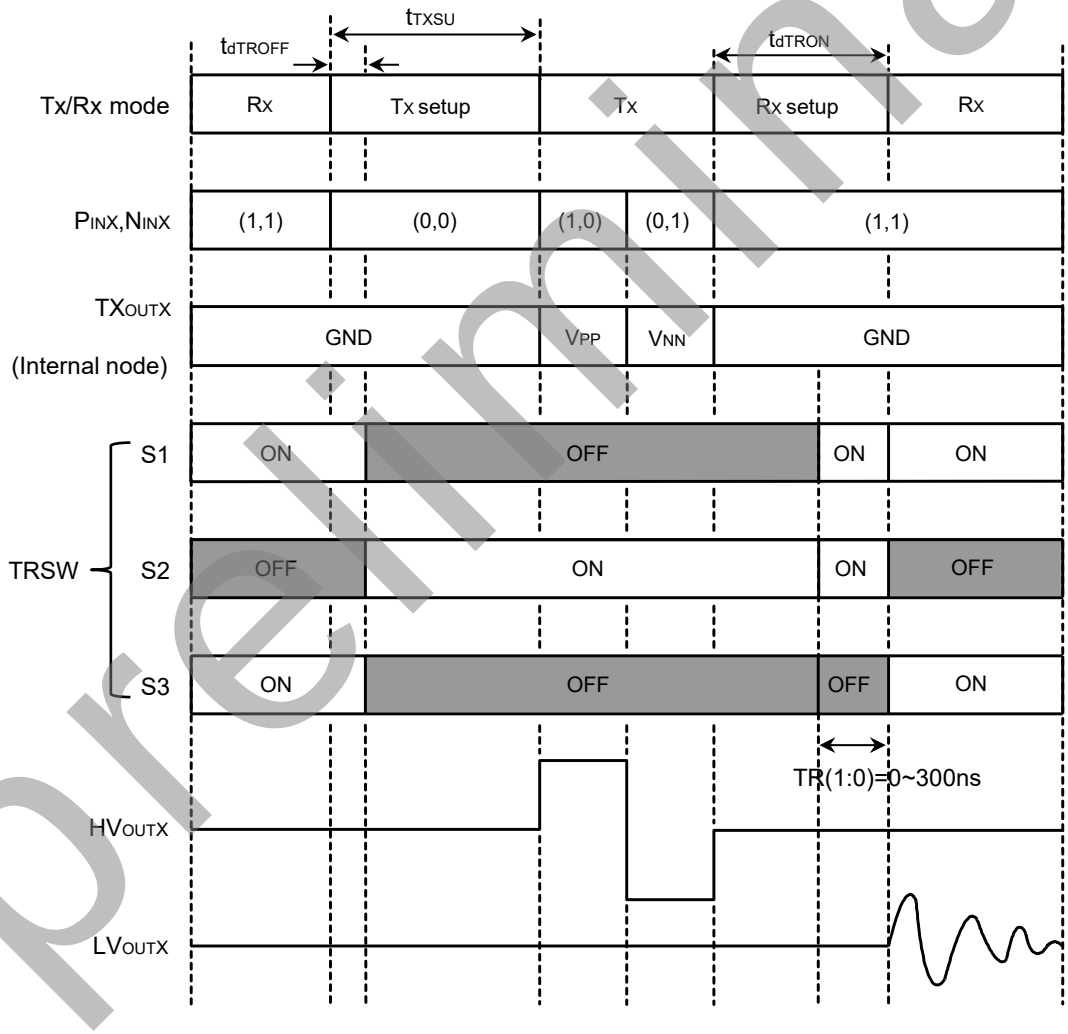

Fig.6 T/R Switch turn-on/off time

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9, Truth Table and Mode Control tables

Table 13 Truth table

Logic Inputs			Internal MOSFET state								Output state	
EN	PINX	NINX	P1	N1	P2	N2	ASW	TRSW			TXOUTX	LVOUTX
			+HV	-HV	GND	GND	GND	S1	S2	S3	(internal node)	
0	0	0	OFF	OFF	**ON**	**ON**	**ON**	OFF	**ON**	OFF	GND	10kΩ
0	0	1	OFF	**ON**	OFF	OFF	OFF	OFF	**ON**	OFF	-HV	10kΩ
0	1	0	**ON**	OFF	OFF	OFF	OFF	OFF	**ON**	OFF	+HV	10kΩ
0	1	1	OFF	OFF	**ON**	**ON**	**ON**	**ON**	OFF	**ON**	GND	HVOUTx
1	X	X	OFF	OFF	OFF	OFF	OFF	OFF	**ON**	OFF	HiZ	10kΩ

Note: VPP/VNN=+/-HV, x=1~8

Table 14 P1/N1 drive current mode

Current Mode	CC1	CC0	PULSER OUTPUT CURRENT (TYP) Iout [A]
0	0	0	0.5
1	0	1	1
2	1	0	1.5
3	1	1	2

Table 15 TRSW S1-S2 turn-on overlap time control mode

TRSW Control Mode	TR1	TR0	S1-S2 ON
			overlap time [ns]
0	0	0	0 (default)
1	0	1	100
2	1	0	200
3	1	1	300

Note: Detailed switching time diagram is shown in Fig.6.

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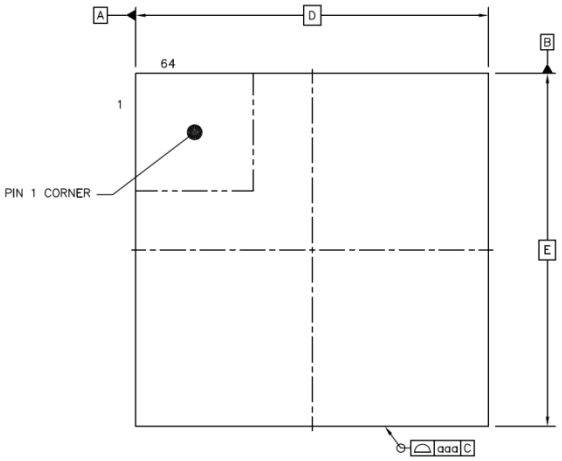
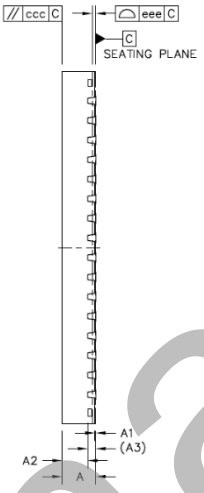
10, 64-Lead QFN Package Outline

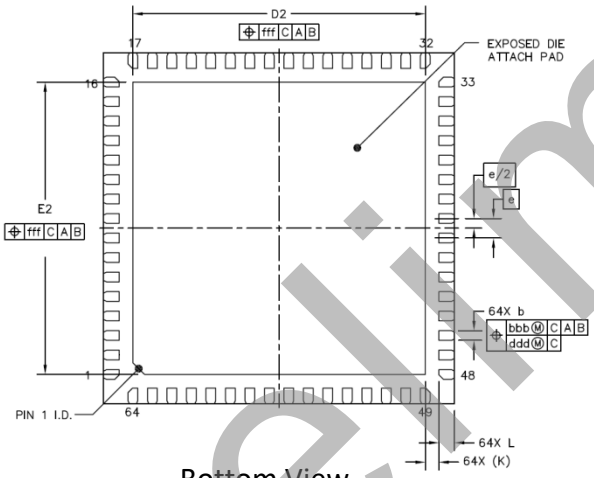
9.00x9.00mm body, 1.00mm height (max), 0.50mm pitch



Top View



Side View



Bottom View

Notes:

Symbol		A	A1	A2	A3	b	D	E	e	D2	E2	L	K	aaa	ccc	eee	bbb	ddd	fff
Dimension (mm)	Min	0.80	0.00	-	0.20 REF	0.20	9.0 BSC	9.0 BSC	0.5 BSC	7.40	7.40	0.30	0.35 REF	-	-	-	-	-	-
	Nom	0.85	0.02	0.65		0.25				7.50	7.50	0.40		0.1	0.1	0.08	0.1	0.05	0.1
	Max	0.90	0.05	-		0.30				7.60	7.60	0.50		-	-	-	-	-	-

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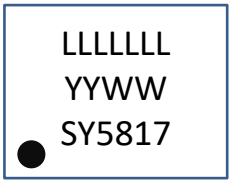
11, Product Marking



L = Lot Number
YY = Year Sealed
WW = Week Sealed

64-Lead QFN

12, Product Identification Information

PART NO.	XX	XX
Device	Package	Media Type

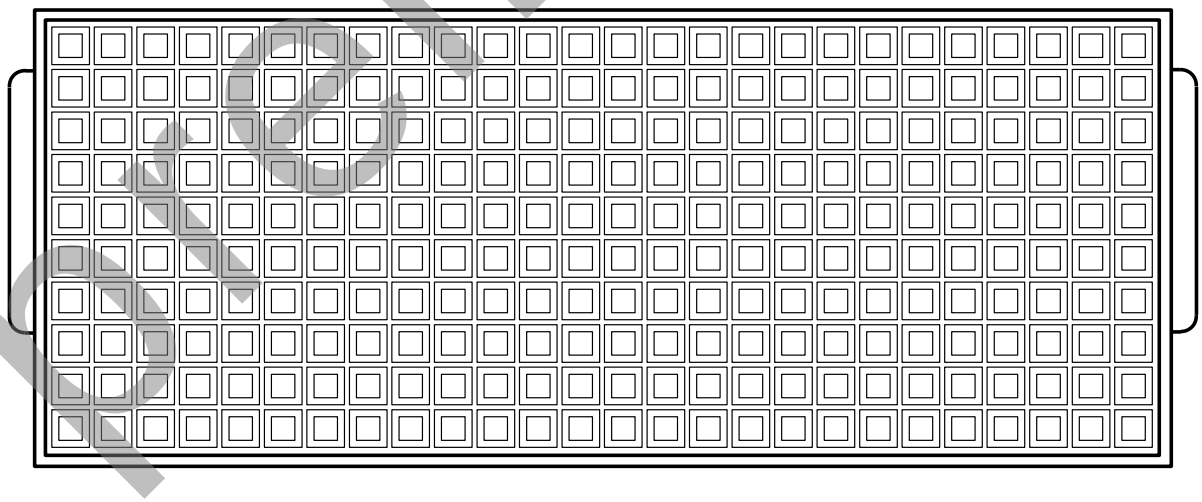
Device: SY5817: 8-Channel 3-Level HV Ultrasound Transmitter with T/R switch

Package: FN: QFN

Media Type: (blank): 2600pcs for MOQ

Examples:

SY5817FN: 8-Channel 3-Level HV Ultrasound Transmitter with T/R switch
64-lead QFN, 9.00x9.00mm
260/Tray x10 for MOQ



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Revision History

Revision #	Revision Date	Pages Updated	Description
Rev 0.0	2025-05-08		Initially released as preliminary specification

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